THE GRSPW SPACEWIRE CODEC IP CORE AND ITS APPLICATION

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Long Paper

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ABSTRACT

SpaceWire based devices are moving rapidly away from just being generic memory mapped interface chips to becoming complex processor-based system-on-a-chip solutions. The function of the SpaceWire link is changing from one being used for high-speed data transfers, to one also being used for remote control and debugging.

There are several key technologies that enable the development of powerful system-on-a-chip designs featuring SpaceWire links and embedded processors. By mastering all of them one can produce new exciting and advanced products for onboard application. This paper will present these key technologies and how they have been utilized in developing an efficient SpaceWire coded that is used in a large set of complex system-on-a-chip designs aimed for the space market.

ENABLING TECHNOLOGIES

With the introduction of the LEON processor family the space community has gained access to a set of powerful 32-bit SPARC V8 based processors that can be targeted towards different FPGA and ASIC technologies. This is the single most important technology required for developing embedded fault-tolerant processing applications.

The adoption of the Advanced Microcontroller Bus Architecture (AMBA) as the on-chip bus fabric used in ESA developments was made simultaneously with the development of the second LEON processor. The standardization has resulted in a multitude of synthesizable cores that are integrated in system-on-a-chip designs.

The SpaceWire Remote Memory Access Protocol (RMAP) allows the implementation of a standardized communication method for reading and writing to remote memory and registers. This eliminates the plethora of existing ad hoc protocols that have been used in previous developments, allowing designers to focus their efforts on a single re-usable solution that can be transferred between projects.

The combination of the RMAP protocol and the Debug Support Unit (DSU), the latter has been developed for the LEON processor family, has opened up the possibility for fast and efficient uploading and remote debugging of software through existing SpaceWire networks, without the penalty of an additional low-speed control bus.

SPACEWIRE CODEC IP CORE

Although the enabling technologies are in place, their efficient implementation is of paramount importance to develop successful products. Gaisler Research has always developed building blocks required for system-on-a-chip design keeping efficiency and compatibility in mind.

The key building block is the GRSPW SpaceWire Codec IP core that has been developed from scratch by Gaisler Research. Contrary to other codec developments, the GRSPW has been designed taking into account from the beginning the previously presented enabling technologies. In addition to implementing the SpaceWire link protocol, the design had to simultaneously meet the constraints posed by the AMBA Advanced High-performance Bus (AHB), providing plug&play capability, full RMAP functionality, tool and technology portability, and finally seamless interaction with the LEON3 and LEON2 processors through the DSU interface.

By taking this overall approach several functions could be combined, for example the data buffering in the front-end codec and direct memory access (DMA) on the AMBA bus, to reduced the size of the core. This has lead to a compact fault-tolerant implementation of the codec IP core that provides full SpaceWire and RMAP functionality and high-throughput using few on-chip resources, making the core suitable for both ASIC and FPGA implementation.

ADVANCED PRODUCTS

The development of advanced building blocks, such as the GRSPW SpaceWire IP core, has resulted in several advanced system-on-a-chip products that are already being shipped to customers.

The first flight products to be shipped to customers are from the LEON3FT-RTAX family. This is an implementation of the LEON3-FT SPARC V8 processor using the Actel RTAX FPGA technology. The fault tolerant design of the IP cores in combination with the radiation tolerant FPGA gives a total immunity to radiation effects. The LEON3FT-RTAX processor is provided in multiple configurations, covering both instrument and spacecraft control applications, and custom configurations are created on request. The configurations offer up to three SpaceWire links with support for implementing RMAP in software.

The first ASIC silicon with LEON3-FT and GRSPW is the GR702RC radiation-hard controller, which has been manufactured on the 180 nm technology from Tower with the objective to assess performance, design flow and radiation behavior of cores using the Ramon Chips' radiation tolerant cell library. The ASIC has been successfully validated and undergone static radiation testing.

The LEON3-FT processor core is being used as the design driver in an ESA activity (1) to validate and qualify the Design Against Radiation Effects (DARE) library, developed by IMEC under ESA founding, on the 180 nm technology from UMC. The ASIC will in addition to the LEON3-FT processor comprise a high-performance floating-point unit, a memory management unit and multiple SpaceWire interfaces with full RMAP support.

The LEON3-FT-MP project has been a preparation for the next generation ESA (2) microprocessor that has the ambition to provide 1,000 MIPS/MFLOPS in a single device. A verification and validation platform, consisting of a multiprocessing system based on the LEON3-FT and GRSPW cores, was successfully developed. Fault tolerant and multi-processing capabilities have been demonstrated and validated.

The planned LEON2-FT AT697F device is equipped with a powerful PCI (Peripheral Component Interconnect) interface, which is ideally suited for interfacing either a back plane bus such as Compact PCI (cPCI) or a companion chip. Gaisler Research has developed the GR701A companion chip that will add amongst others multiple SpaceWire interfaces, using the GRSPW core, to the AT697F device.

The GRSPW core is also being used in the SpaceWire test equipment developed by Gaisler Research. The GRESB Ethernet to SpaceWire bridge is internally based on a Xilinx FPGA implementing a system-on-a-chip design featuring LEON3 and multiple GRSPW cores. The GRESB allows communication with SpaceWire links through Ethernet, supporting functions such as SpaceWire packet routing, IP tunneling, remote debugging of LEON3 and LEON2 processors, etc.

There are several more system-on-a-chip developments in progress using the LEON3-FT and GRSPW cores, made both in-house and by customers, of which many cannot be disclosed at this point in time.

CONCLUSIONS

By embracing the enabling technologies presented in this paper several powerful system-on-a-chip designs have been developed in a short period of time. The key factors have been efficient implementation of truly re-usable IP cores, such as the GRSPW SpaceWire codec, which have been designed with interoperation and portability in mind from the start. This has resulted in sophisticated flight products that are being shipped to customers.

Footnotes

(1) ESA Contract Number 19916/06/NL/JD

(2) ESA Contract Number 18533/04/NL/JD