

DESIGN AND IMPLEMENTATION OF SYNTHESIZABLE SPACEWIRE CORES

Session: SpaceWire Components

Short Paper

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ABSTRACT

The Space Research Group of the University of Alcalá is currently developing a library of IP cores in order to provide main space systems and subsystem SoC implementation. The idea behind is to have an independent set of synthesizable device cores which can be easily optimized using device embedded resources such as PLL, DLL or memory blocks (RAM or ROM) to improve area or timing constraints.

One of these IP cores is an ECSS-E-50-12A based SpaceWire core covering the whole standard specification in two different approaches: a basic implementation, consisting in a basic node codec (up to the standard exchange level), and a extended core, offering a whole router core made from former codec plus the standard network and packet level implementation. Our goal is to achieve a technology independent synthesizable core supporting the highest standard data rate, 400 Mbps, optimized for timing and area as far as possible.

In this paper, a brief description of the developed SpaceWire cores, together with the synthesis and timing simulation results, are presented. The presented cores have been synthesized on devices from different families of FPGAs (SRAM, flash and antifuse based FPGA). The results obtained are compared with other existing core results in order to evaluate the accuracy of the design. After improving the synthesis results adding internal FPGAs resources such as PLL to avoid external resources dependence (mainly clock), the resulting programming file is tested on different devices to check the post layout simulation results against a real performance example in a running FPGA.