

SPACEWIRE ROUTER ASIC

Session: SpaceWire Components

Short Paper

Steve Parkes ¹, Chris McClements ¹, Gerald Kempf ², Stephan Fischer ³,
Agustin Leon ⁴

¹*School of Computing, University of Dundee, Dundee, DD1 4HN, Scotland, UK.*

Email: sparkes@computing.dundee.ac.uk.

²*Austrian Aerospace*

³*Astrium GmbH*

⁴*European Space Agency*

ABSTRACT

A SpaceWire routing switch is able to connect together many nodes, providing a means of routing packets between the nodes connected to it. A SpaceWire routing switch comprises a number of SpaceWire link interfaces and a routing matrix. The routing matrix enables packets arriving at one link interface to be transferred to and sent out of another link interface on the routing switch.

A radiation tolerant routing switch is currently being developed which has the following facilities:

- Eight SpaceWire ports.
- Two external parallel ports, each comprising an input FIFO and an output FIFO.
- A non-blocking crossbar switch connecting any input port to any output port.
- An internal configuration port accessible via the crossbar switch from the external parallel port or the SpaceWire ports.
- A routing table accessible via the configuration port which holds the logical address to output port mapping.
- Control logic to control the operation of the switch, performing arbitration and group adaptive routing.
- Control registers than can be written and read by the configuration port and which hold control information e.g. link operating speed.
- An external time-code interface comprising tick_in, tick_out and current tick count value.
- Internal status/error registers accessible via the configuration port
- External status/error signals

The SpaceWire Routing device is currently being manufactured by Atmel.

The full paper will describe the main features of the SpaceWire Router device and its architecture. The results of extensive testing on an initial FPGA prototype will be reported. Finally the anticipated performance will be provided.