A SPACE WIRE IMPLIMENTATION OF CHAINLESS BOUNDARY SCAN ARCHETECTURE FOR EMBEDDED TESTING

Session: SpaceWire onboard equipment and software embedded

Short Paper

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Electronic equipment for complex digital payloads have become increasingly more sophisticated incorporating thousands of ASICs with intensive interconnect between them. Most of these ASICs have to be monitored and controlled to satisfy the mission operational requirements. One scheme for implementing this is by connecting all these ASICs using a reliable network and interconnect such as SpaceWire. The ASIC in the system act as nodes which include their own SpaceWire routers. The testing and validation of the all electrical interconnects in such a complex system becomes a major contributor to increasing the schedule and cost of a project. Therefore built in self test, embedded test, strategies have been employed to alleviate these issues.

Traditionally IEEE Std 1149.1 (JTAG) – Boundary scan - testing standard has been used to implement embedded test. Components in the system have to be daisy chained and driven by the JTAG control bus in parallel. Such an architecture has a number of limitations: Firstly, a faulty ASIC within a daisy chain will prevent testing of the whole chain. Secondly the parallel JTAG control bus puts undesirable constraints on the design of reliable systems. To overcome these limitations, and make the boundary scan test infrastructure transparent and independent of the design of the system under test, a generic chainless boundary scan architecture have been developed. This architecture is well suited to systems which use SpaceWire networks.

This paper proposes a dual function for the SpaceWire network. One, to facilitate the performance of embedded test. The other, is its standard role in communicating data and commands between nodes. A UK patent application has been filed covering the method, architecture and technology described in this abstract.