A METHODOLOGY AND THE TOOL FOR TESTING SPACEWIRE ROUTING SWITCHES

Session: SpaceWire test and verification

Short Paper

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ABSTRACT

SpaceWire routing switches could include functions of multicasting and adaptive routing. But supporting of these functions essentially complicated verification and testing process.

The article presents the developed test shell for verification and parameter evaluation of routing switches with different number of ports and for networks with different topology and number of switches; for data packet flows automatic generation with different parameters. Also the test shell could be used for testing of RTL models and post-synthesis netlists.

We use SystemC and Cadence SimVisio design tools for these test shell development. SystemC provides development of parameterized models with flexible behavior. SimVisio tools allows integration of mixed language models (SystemC, VHDL, Verilog) in one project.

A network model is represented by the parametrized shell that includes models of SpaceWire routing switches, terminal nodes, interconnection lines, and a control and monitoring block. When a user specifies parameters (number of nodes, switches, intersonnection topology, and other parameters) the shell configures the network model automatically. Users could apply this model for verification and parameter evaluation of his SpaceWire routing switches. The control and monitoring block performs simulation control (initialization of routing switches and terminal nodes, starts data transmission, global result checking). The models of the shell, routing switches, terminal nodes, interconnection lines, and a control and monitoring block are written in SystemC. RTL routing switches models on VHDL or Verilog and netlists (VHDL, Verilog) also could be used.