SPACEWIRE IP FOR ACTEL RADIATION TOLERANT FPGAS

Session: SpaceWire Components

Short Paper

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ABSTRACT

STAR-Dundee Ltd and University of Dundee have teamed with Actel to provide a range of SpaceWire IP cores optimised for the Actel RTAX-S radiation tolerant series of devices [1]. FPGA technology is ideal for instrument development, allowing one off equipment development without the large non-recurring engineering (NRE) costs of ASICs. The RTAX-S family provides a large number of available logic gates enabling complete instrument interface and control systems to be integrated on a single device.

SpaceWire [2] [3] was designed to provide a fast and efficient (low gate count) interface suitable for use onboard spacecraft. It is now being widely used by the major space agencies and aerospace industry across the world. SpaceWire is ideal for connecting an instrument into an onboard data-handling system and many missions are now selecting SpaceWire as the onboard interface of choice.

A ready laid-out SpaceWire interface with guaranteed timing, that fits into a corner of an Actel RTAX-S device would make the design of instrument interface and control FPGAs much simpler. Effort could then be concentrated on the application specific design without having to be concerned about the SpaceWire interface design.

The Actel "Block Flow" technology makes this possible. A functional block with fixed layout can be integrated with general user logic. STAR-Dundee are designing a series of SpaceWire interface blocks including a SpaceWire interface and a SpaceWire interface with Remote Memory Access Protocol (RMAP) support [4] and a SpaceWire router. The first of these IP blocks will be available in 4Q 2007.

SPACEWIRE RMAP IP ARCHITECTURE

The SpaceWire IP will be derived from the CODEC developed by University of Dundee for ESA [5], adapted to suit the Actel FPGA devices. The target is for this to operate at up to 200 Mbits/s in an Actel RTAX device. Time-codes will be supported in the SpaceWire interface.

The RMAP IP will again be tailored to the Actel devices. The architecture for a slave SpW/RMAP IP core is illustrated in Figure 1.

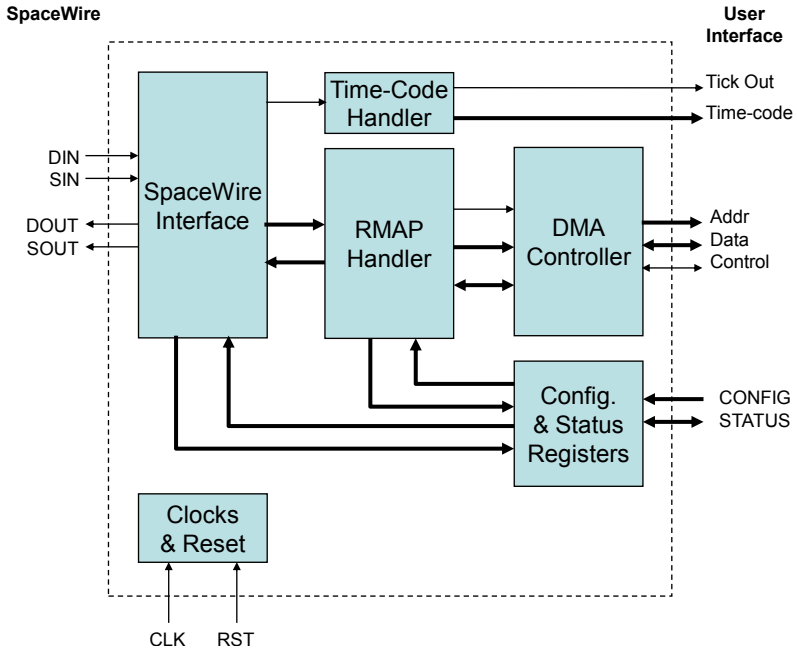

Figure 1 SpW/RMAP Interface Architecture

The SpaceWire Interface is responsible for receiving SpaceWire packets and time-codes and passing them to the RMAP Handler and Time-Code Handler respectively. It also transmits SpaceWire packets when requested to do so by the RMAP handler. The packets it sends are RMAP reply or acknowledgement packets.

The Time-Code Handler is responsible for checking time-codes and maintaining the value of the time-code counter. It will assert the TICK_OUT signal when a valid time code is received and put the value of each valid time-code on the TIME-CODE output.

The RMAP Handler is responsible for checking and responding to valid RMAP packets. It will set up the DMA controller to perform reads and writes to user memory and registers and will form the reply or acknowledgement to the RMAP command for sending by the SpaceWire interface.

The DMA controller provides the interface to user memory and registers. It is responsible for gaining access to the user data bus and performing memory or register, read or write operations.

The Configuration and Status registers hold configuration and status information for the SpaceWire interface and RMAP Handler. On power up certain configuration registers are loaded with default values specified by the CONFIG interface. Thereafter the configuration values may be changed by writing to the configuration registers either by a SpaceWire-RMAP command or by the user logic writing to the appropriate registers. Status information from the SpaceWire interface and RMAP Handler is held in status registers which can be read by SpaceWire-RMAP command or by the user logic. Certain status information is also available on dedicated signals, STATUS, from the SpW/RMAP IP core.

The Clock and Reset block is responsible for providing the user reset signal, RESET, to the relevant parts of the SpW/RMAP IP core ensuring a clean condition after the reset signal has been asserted. It is also responsible for generating any necessary clock signals from the single clock input signal, CLK.

An example sequence diagram for handling an RMAP verified write command with acknowledgement is given in Figure 2.

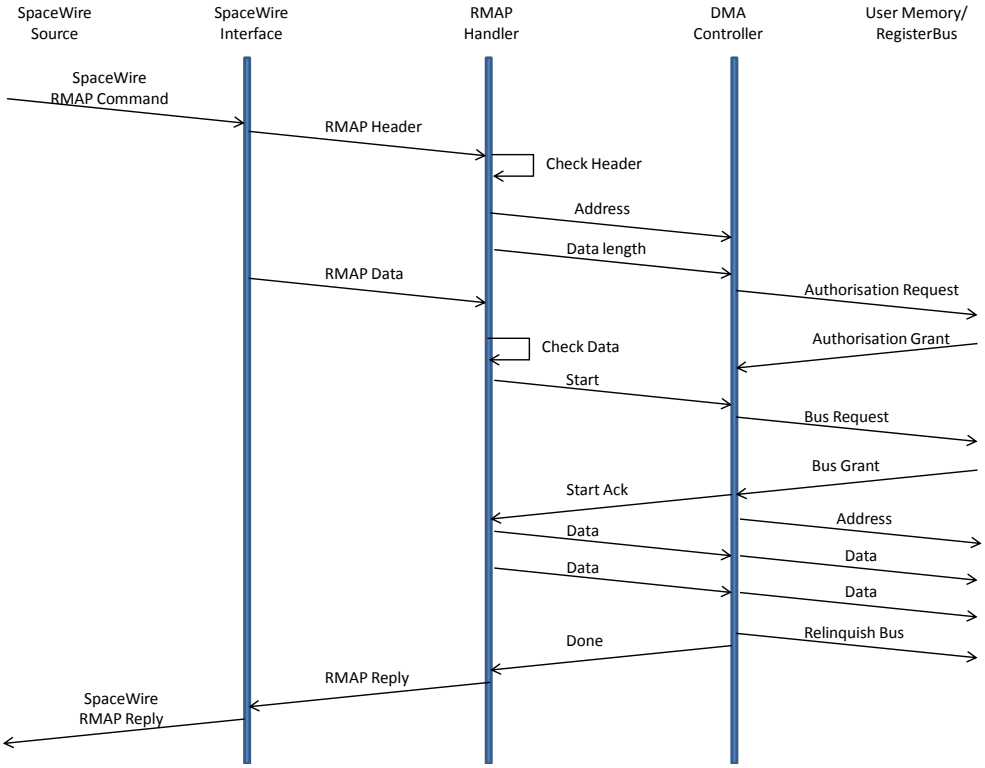

Figure 2 Sequence Diagram for RMAP Verified Write

The SpaceWire packet containing the RMAP write command arrives at the SpaceWire interface and is passed on to the RMAP handler. The RMAP header arrives character by character at the RMAP handler and is decoded and checked for errors. Assuming that there are no errors the address to write to and the amount of data to be written are passed to the DMA controller. The DMA controller checks with the user logic that it is authorised to write to this area of memory.

In the meantime the data has arrived at the RMAP handler it is buffered and the data CRC checked to make sure that the data is without error. The RMAP handler then tells the DMA controller to start writing the data to the specified area of user logic memory. The DMA controller requests use of the user bus and when granted access will transfer the data from the buffer in the RMAP handler to the user logic memory. Once the data has been transferred the user bus is relinquished and the RMAP handler is told that the DMA transfer is complete.

The RMAP handler now forms the RMAP reply with the status field set to zero to indicate success. This is sent back to the source of the original RMAP command by the SpaceWire interface.

CONCLUSIONS

An IP core containing a well proven SpaceWire CODEC with added RMAP support will be available for use in a radiation tolerant FPGA with fixed placement to ensure the timing. This will be a valuable addition to the current range of SpaceWire components.

REFERENCES

[1] Actel RTAX FPGA website http://www.actel.com/products/milaero/rtaxs/

[2] European Cooperation for Space Standardization, Standard ECSS-E-50-12A, "SpaceWire, Links, Nodes, Routers and Networks", Issue 1, European Cooperation for Space Data Standardization, January **2003**.

[3] European Space Agency, "SpaceWire Web Page", European Space Agency, http://spacewire.esa.int/

[4] Parkes S.M. et al, "Remote Memory Access Protocol", ECSS-E50-11 draft F, December 2006.

[5] ESA IP Cores http://www.esa.int/TEC/Microelectronics/SEMVWLV74TE_0.html

[6] STAR-Dundee Website www.star-dundee.com