A SYSTEM-ON-CHIP RADIATION HARDENED MICROCONTROLLER ASIC WITH EMBEDDED SPACEWIRE ROUTER

Session: SpaceWire Components

Long Paper

Richard Berger, Laura Burcin, David Hutcheson, Jennifer Koehler, Marla Lassa, Myrna Milliser, David Moser, Dan Stanley, Randy Zeger

BAE Systems, 9300 Wellington Road, Manassas, Virginia 20110 USA

Ben Blalock, Mark Hale

University of Tennessee, 1508 Middle Way Drive, Knoxville, Tennessee 37996 USA

E-mail: richard.w.berger@baesystems.com, laura.burcin@baesystems.com, david.hutcheson@baesystems.com, jennifer.koehler@baesystems.com, marla.lassa@baesystems.com, myrna.milliser@baesystems.com, dave.moser@baesystems.com, dan.stanley@baesystems.com, randy.zeger@baesystems.com, bblalock@ece.utk.edu, mhale1@utk.edu

ABSTRACT

A mixed-signal radiation hardened computer ASIC that includes a four port SpaceWire router is currently in development. Based on the RAD6000™ microprocessor currently flying on numerous space missions and commanding the Mars Exploration Rovers, this massively integrated system-on-chip is capable of performing flight computer and instrument controller functions and can reuse existing RAD6000 software and test infrastructure. The ASIC will be manufactured in a 150nm radiation hardened CMOS technology. Initiated in 2005 as a NASA technology project, development has continued with funding from the Air Force Research Laboratory's Space Vehicles Directorate, Kirtland Air Force Base, N.M..

The ASIC incorporates an enhanced version of the reusable SpaceWire router core with four SpaceWire links and dual internal ports that was previously created for the BAE Systems SpaceWire ASIC. This newer version reduces both die area and power dissipation while improving link performance. The ASIC employs a flight-proven reusable core architecture with a common bus medium. In addition to the RAD6000 microprocessor and SpaceWire cores, the ASIC includes a pipelined 12-bit A/D converter with a programmable multiplexer, three channels of 12-bit D/A conversion, 192KB of on-chip SRAM, 32KB of chalcogenide-based C-RAM™ non-volatile memory, a 64-bit PCI interface, a 1553 interface, a DMA controller, and an external memory controller. A 2nd smaller microcontroller core called the EMC has also been incorporated on the ASIC. It is supported by a compiler developed by BAE Systems and software supporting the SpaceWire transport layer has already been developed.

This paper discusses the architecture and functions of the microcontroller ASIC, including the SpaceWire core implementation and features. Operational configurations matched to a variety of applications will also be shown.

Approved for public domain release (VS07-0571) ©2007 BAE Systems All rights reserved

INTRODUCTION TO THE RAD6000MC™ MICROCONTROLLER

Based on the BAE Systems flight-proven RAD6000™ microprocessor and integrating a wide variety of digital and analog interfaces and both SRAM and non-volatile memory, the RAD600MC is a true system-on-a-chip. It is being designed for a variety of applications that include both flight computer processing and instrument control. It supports both legacy buses such as MIL-STD-1553 and the rapidly growing SpaceWire serial bus through an integrated four-port router with dual internal interfaces. The RAD6000MC also supports up to 48 analog input channels, making it ideal for interface with spacecraft sensors and includes three channels of D/A conversion. Non-volatile memory is implemented with a new embedded C-RAM memory macro. Much of the RAD6000MC design is reused from ASICs already proven in hardware and/or currently in development, decreasing both the design cost and risk associated with the program. The ASIC will be manufactured in a radiation hardened 150nm CMOS technology.

RAD6000™ MICROPROCESSOR BACKGROUND AND CORE TRANSLATION

Originally developed by IBM in 1990 as the first single chip implementation of the RISC System/6000 "Power" architecture [1] and the predecessor to the PowerPC line of microprocessors, the RAD6000 microprocessor [2] was created in 1995 in a 0.5 micron radiation hardened CMOS technology by modifying the circuitry for reliable spaceborne operation. This processor was quickly adopted and has been employed in many NASA missions as the flight computer, as well as the command processor in both generations of the Mars rovers. As shown in Figure 1, the RAD6000 central processor unit (CPU) includes both fixed point and floating point execution units in a superscalar RISC architecture executing up to three instructions per cycle. A two-way set associate unified 8 KB cache memory is also included. The existing microprocessor component is capable of operation at up to 33 MHz, with a throughput of 35 MIPS. The processor was originally developed using IBM's proprietary design languages and design tools. Separate buses are provided for I/O and memory. The RAD6000 is supported by the VxWorks real time operating system from WindRiver and a Green Hills C Compiler. Diagnostics are supported using the RAD6000's Common On-Chip Processor (COP) function.

When ported to a 150nm CMOS technology, the RAD6000 decreases in size by almost six times, making it quite viable for use as an embedded processor core. However, there were several steps required to bring that to fruition. The first step was to translate the logic design into VHDL to create a model compatible with industry-standard simulation tools that would ease simulation with other cores. The translated model was validated both with functional simulations and simulations of the original design's manufacturing test patterns. All existing Interfaces and the original Level Sensitive Scan Design (LSSD) latches were maintained in order to allow validation post-manufacturing using the current test patterns as well.

The COP function was enhanced with the addition of a slave interface to the On Chip Bus [3] to complement the existing off-chip interface for connection to existing RAD6000 diagnostic tools. This change will allow access to the COP from the JTAG cores as an alternative diagnostic approach.

Approved for public domain release (VS07-0571) ©2007 BAE Systems All rights reserved

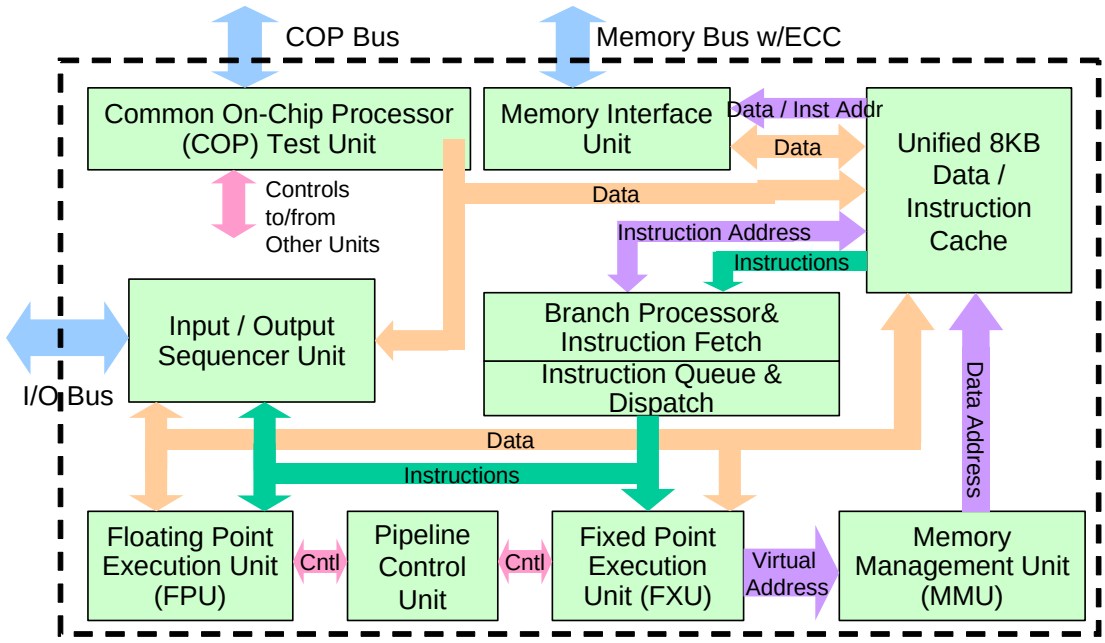


Figure 1: RAD6000 Microprocessor Architecture

The next important step was to develop an interface between the RAD6000 processor and the On-Chip Bus connection medium employed with all of BAE Systems' core-based designs. The original bridge ASIC developed for the standalone RAD6000 microprocessor was called the LIO ASIC. It was determined that while the key functions of the LIO were needed, a direct translation of the LIO into a core was not appropriate.

The Local Interface Function (LIF) core was designed specifically for this purpose. It provides direct connections to both the I/O bus and memory bus of the RAD6000, direct connection to the newest version of the external memory controller core, and three direct connections to the On-Chip Bus (OCB). The LIF is implemented as a set of sub-cores as shown in the block diagram in Figure 2, connected by a cross-bar switch to minimize contention for its many interfaces. In addition to the typical master and slave interfaces to the OCB, the LIF features a second slave interface designed to allow other cores to access external memory without interfering with the operation of the microprocessor.

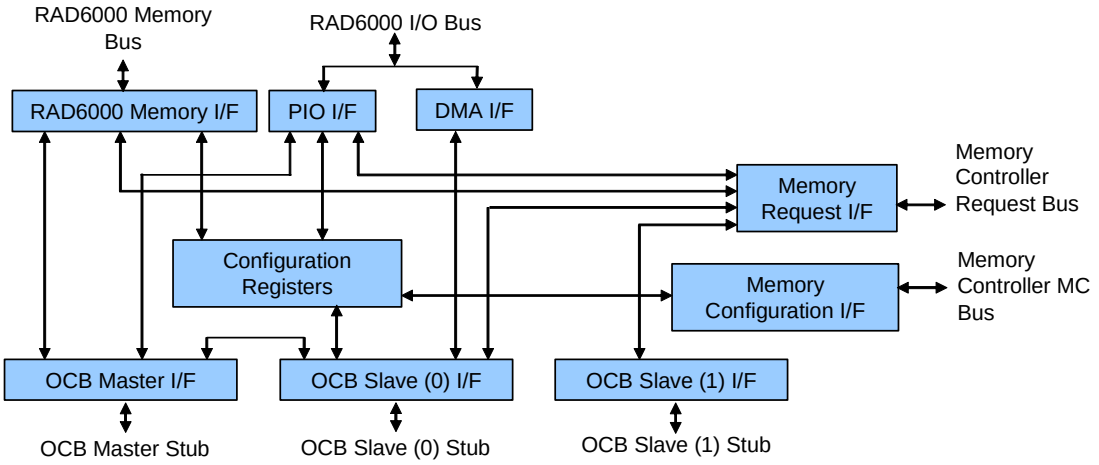


Figure 2: Local Interface Function Core Block Diagram

Approved for public domain release (VS07-0571) ©2007 BAE Systems All rights reserved

The two slave interfaces are used to partition the address space, which has been massively expanded beyond that supported by the standalone processor chip. The memory address bus of the RAD6000 was 27 bits, corresponding to 128 MB of addressable memory. The LIF extends that to 32 bits through address translation, as shown in Figure 3. The uppermost three bits are used to select one of eight 16 MB pages whose base address is stored in base address registers. The memory address map is defined to provide a total of 2 GB of RAD6000 address space. The other 2 GB of the 4 GB total address space is dedicated for use by the other cores that reside on the On Chip Bus.

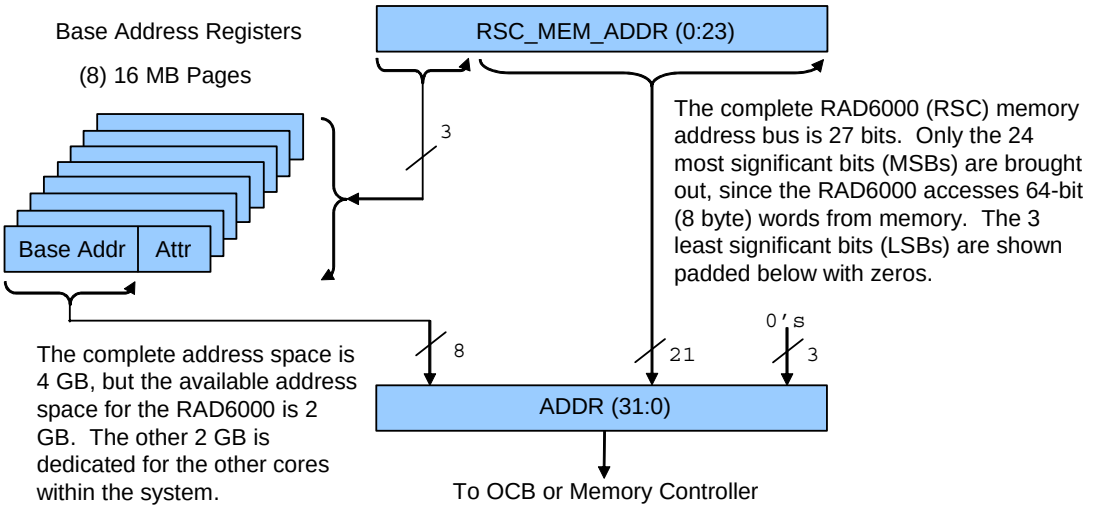


Figure 3: RAD6000 Memory Address Translation

In the LIF, only the first OCB slave (0) interface is used for the 128 MB of memory that corresponds to the original address space. When the memory access from the OCB falls within the original 128 MB RAD6000 memory address space, the interface accesses the base address registers and supports cache snooping if required. This operation is shown in Figure 4. The second OCB slave (1) interface does not support the original 128 MB of memory. It has no connection to the cache and is designed to support high speed direct access of memory by other cores through the OCB.

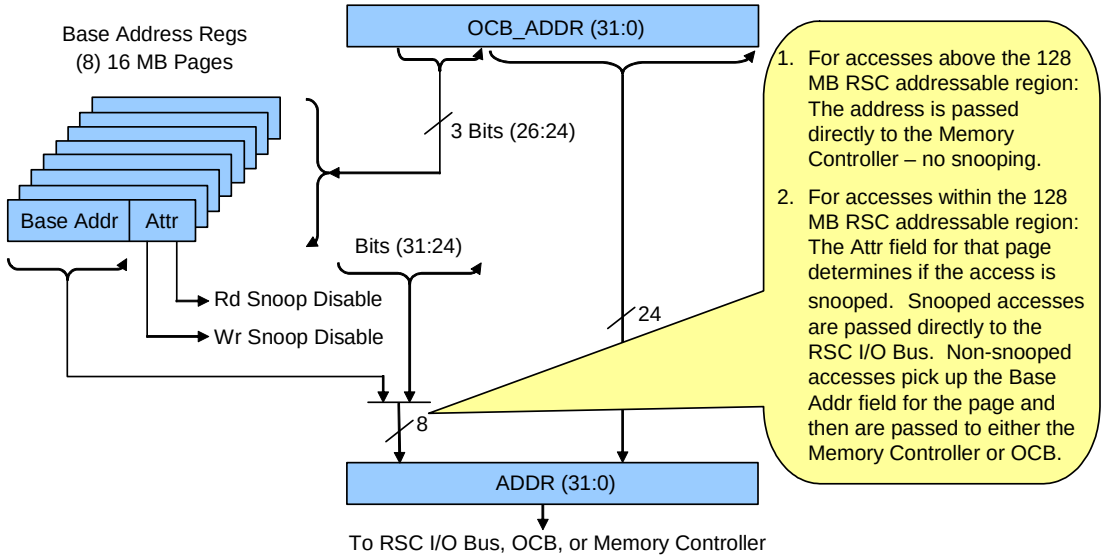


Figure 4: OCB Slave Address Translation

Approved for public domain release (VS07-0571) ©2007 BAE Systems All rights reserved

External memory is accessed by a memory controller core connected to the LIF. The core provides for two different types of error correction, single bit correction with double bit detection (SECDED) and nibble-level error correction. It can support a combination of SRAM, SDRAM, and non-volatile memory.

ON-CHIP BUS CONNECTION MEDIUM

The On-Chip Bus (OCB) is the standard connection medium used with all of BAE Systems' reusable cores and is the central element of the reusable core architecture [3]. It consists of two data buses configured as a crossbar switch that prevents contention between cores unless multiple cores are trying to access the same destination simultaneously. The high speed data bus is 64 bits and the low speed bus is 32 bits, connected by an internal OCB bridge. The higher speed data bus includes word level parity. The lower speed bus supports word, half-word, and byte parity. There is a separate 32-bit address bus, also with parity at the word level.

Connection between the OCB and reusable cores is provided by standard Master and Slave OCB "stub" logic. An OCB bus transaction consists of an address phase that begins with a request issued by the Master stub, followed by a data phase once the Slave has acknowledged the request. Once the request is acknowledged, optimum bus utilization is achieved through the use of address and data pipelining. In the OCB configuration for the RAD6000MC microcontroller ASIC, the higher speed bus has 11 master and 9 slave stub connections. The lower speed bus includes a single master with 9 slaves. This is shown on the RAD6000MC block diagram in Figure 5.

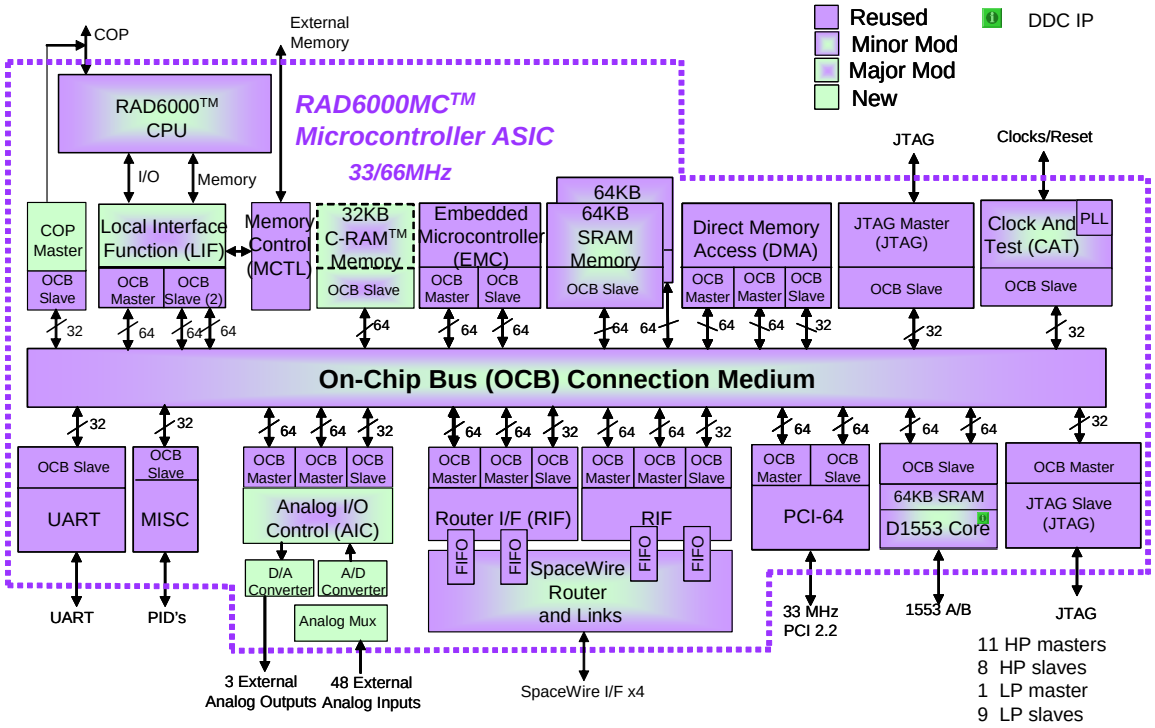


Figure 5: RAD6000MC ASIC Block Diagram

Approved for public domain release (VS07-0571) ©2007 BAE Systems All rights reserved

DIGITAL BUS INTERFACES

The RAD6000MC supports three digital bus interfaces that offer the user tremendous flexibility in implementation. For high reliability serial interfaces with low throughput requirements, a MIL-STD-1553 interface is supported. This interface is based on a synthesizable core from Data Device Corporation (DDC), a well-known provider of certified 1553 components. It supports Bus Controller and Remote Terminal (BC/RT) functions and provides dual redundant links. The 1553 interface includes a dedicated 64 KB SRAM memory block. If the 1553 interface is not being used, the user can treat the 64 KB SRAM as a third block of memory usable by the RAD6000 microprocessor or any of the other cores.

The SpaceWire interface is based on a router and serial link design originally developed for NASA Goddard Space Flight Center (GSFC), with features specific to the BAE Systems implementation currently in production in the BAE Systems SpaceWire ASIC [4]. The router includes four external links and two internal interfaces to the OCB via dual Router Interface (RIF) cores that minimize the risk of internal bottlenecks, as shown in Figure 6. The links have integrated LVDS drivers and receivers with cold sparing support. A unique bypass mode allows a fixed routing assignment, improving throughput in cases where the routing location is always known. A maximum packet length feature minimizes the chance of network stalling. This second generation version of the core also decreases the die area required for the router and operates it at a higher clock rate, improves performance of the time code function, and operates at a higher link rate (300 Mbps) when implemented in 150nm CMOS technology.

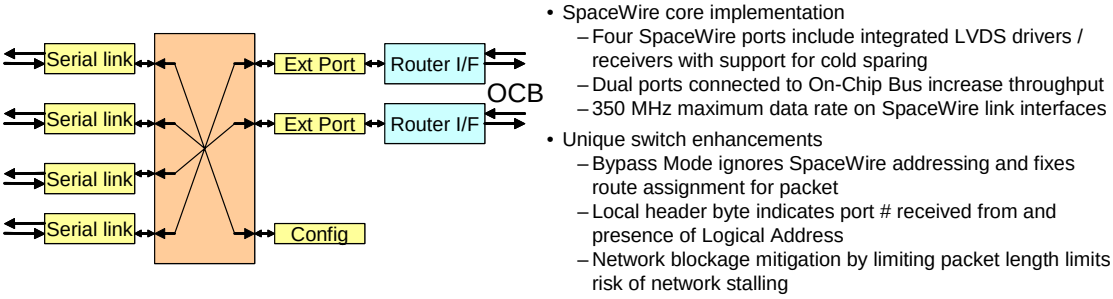


Figure 6: SpaceWire Links and Router With Dual On-Chip Bus Interfaces

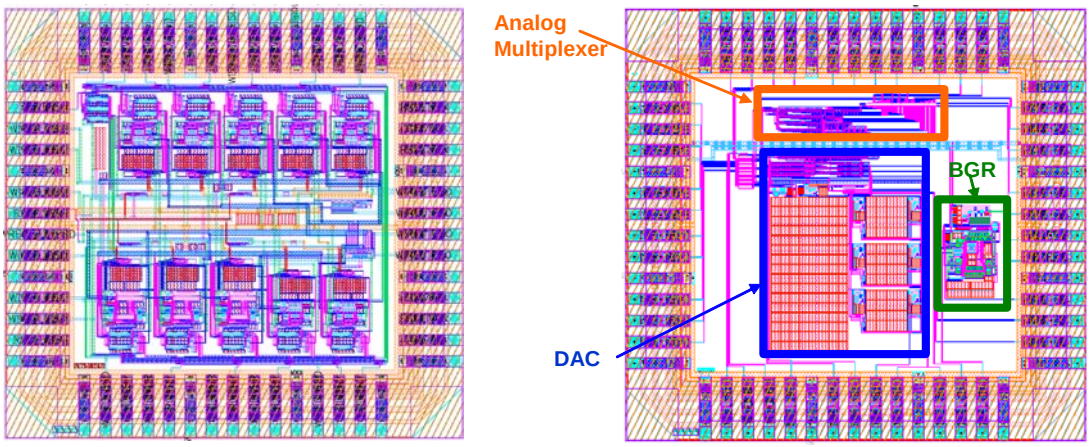
High throughput parallel data transfers are supported by a 64-bit Peripheral Component Interconnect (PCI) bus (version 2.2) interface that can operate at up to 66 MHz on a board or at 33 MHz across a CompactPCI backplane. Bus throughput @ 33 MHz is up to 264 MB per second. The PCI interface includes word level parity on the 32-bit address bus and on both words of the 64-bit data.

ANALOG CIRCUITS AND INTERFACE CORE

The RAD6000MC includes a 12-bit Analog-to-Digital converter (ADC) operating at 8.25 Msps, with a matching programmable analog multiplexer and differential output Bandgap Reference (BGR) circuit. The ADC implements a 1.5-bit per stage pipeline architecture that is capable of sampling rates up 10 Msps at full resolution. It accepts a 4 volt, fully differential input. A high accuracy sample and hold circuit is incorporated into the ADC. The circuit includes a folded-cascode amplifier with four high-gain Operational Transconductance Amplifiers used as regulation amplifiers to

Approved for public domain release (VS07-0571) ©2007 BAE Systems All rights reserved

enhance gain and minimize propagation of errors through the stages of the ADC. A digital error correction algorithm is employed so that comparator errors up to 500 mV can be tolerated.



Pipeline A/D Converter test chip

Wilkinson D/A Converter, analog multiplexer, and Bandgap Reference test chip

Figure 7: Analog/Digital Converter and Digital/Analog Converter Test Chip Layouts

The entire ADC function was designed with 3.3 volt transistors. This provided for the highest dynamic range on analog inputs and resulted in lower power dissipation, rated at 200 mW. If the ADC is not being used, bias to the sample and hold amplifiers can be disabled via a small PMOS transistor within the current mirror of the A/D converter's current bias circuit to reduce power. The ADC has been manufactured on a test site and hardware is currently being tested. The circuit occupies 4.4 square millimeters (sq. mm.) of silicon, as shown in Figure 7.

The accompanying programmable analog multiplexer has been designed to support up to 48 single end inputs, up to 24 differential inputs, or limited combinations of both (8 differential and 32 single ended or 16 of each) to provide users with maximum flexibility. Area of the multiplexer circuit is 0.75 sq. mm.

The Bandgap Reference (BGR) circuit provides the differential reference voltage required by the ADC. Designed with continuous-time common-mode feedback, the BGR is very stable across the mil-spec temperature range varying by only 12 mV in simulations. Estimated power dissipation is 48 mW and circuit area is 0.27 sq. mm.

The D/A converter circuit is based on a novel Wilkinson architecture that dissipates only 5.5 mW at a 1 Ksps conversion rate and occupies a moderate silicon area of 1.54 sq. mm. while providing three channels of 12-bit resolution. The Wilkinson architecture minimizes the area increase for multiple channels by employing a shared ramp generator and pipelined Gray code digital counter with a 4.125 MHz clock. The track and hold circuits for each channel track the ramp generator voltage until it receives a pulse sent from the matching comparator. The track and hold amplifier then holds that analog value until the next voltage conversion.

All three of these circuits have been released on a test chip that is currently in manufacturing, shown in Figure 7. Hardware is expected by the end of 2007.

Approved for public domain release (VS07-0571) ©2007 BAE Systems All rights reserved

Connection of the analog circuitry to the OCB is achieved with the Analog I/O and Control (AIC) reusable core. This function provides the clocks and control signals required by all of the analog circuits. A set of six select bits is used to program the multiplexer.

EMBEDDED C-RAM NON-VOLATILE MEMORY AND ON-CHIP SRAM MEMORY

The 32 KB chalcogenide-based C-RAM macro is the first implementation of an embedded C-RAM core, adapted from BAE Systems' 4 Mb, C-RAM non-volatile memory chip [5]. The principle behind chalcogenide-based non-volatile memory is that of phase change. Current is applied to change a small quantity of chalcogenide material that represents the memory bit storage node between the amorphous and crystalline states, thereby achieving "0" and "1" stored values. Organized as 1,024 words by 32 bits, this core was sized specifically to provide built-in start-up ROM functionality for the RAD6000 that requires 26 KB of memory. The core is currently in manufacturing and testing will be performed late in 2007. A version of the macro with embedded error correction code (ECC) is now being designed to enhance manufacturing yield.

There are two 64 KB SRAM memory macros directly connected to the OCB. Splitting them allows multiple cores to access blocks of memory simultaneously across the OCB, taking advantage of the crossbar switch architecture. A third 64 KB SRAM resides within the 1553 core, and is dedicated to that interface when it is in operation. However, when the 1553 interface is not required, the user can reallocate it as a third generally available on-chip memory core.

EMBEDDED MICROCONTROLLER

In addition to the RAD6000, the microcontroller ASIC includes a smaller processor called the Embedded Microcontroller (EMC) [6]. The EMC is a synthesizable, 32-bit RISC processor with moderate throughput, based on a BAE Systems architecture and instruction set. It incorporates a 2 KB instruction cache and is supported its own C compiler, also developed by BAE Systems. Executing a single fixed point instruction per cycle, the EMC is employed to control reset sequences for the RAD6000, for housekeeping functions, and for support of some reusable cores. As an example of this, code has already been written in support of the SpaceWire interface, creating descriptors to partition large data files to provide a more manageable downlink.

CONFIGURABILITY FOR VARIOUS APPLICATIONS

The RAD6000MC will be configurable as required for various applications through a series of personalizations. RAD6000 processor clock speed will be selectable for either 33 or 66 MHz, emphasizing throughput vs. power dissipation. Clocking to the various interface cores may be gated to decrease power dissipation, if they are not required for a specific application; although some functions must always be operational. As mentioned above, one 64 KB memory macro may be used either dedicated to the 1553 bus or made available for general use. Additional external memory may be added where required.

Shown in Figure 8 in an example of a specific operation as part of a larger distributed computing system, the microcontroller is operating a robotic arm in a system that is

Approved for public domain release (VS07-0571) ©2007 BAE Systems All rights reserved

based on distributed computing. In this example, communication and data transfers occur across the SpaceWire network. Analog control of the joints of the arm would be achieved through use of the D/A converters. Tactile feedback via sensors would be transmitted through the multiplexer and A/D converter. As a subsystem with limited functions, a robust operating system is probably not required, so a microkernel can be employed. This likely eliminates the need for external memory, making the microcontroller completely self-contained. Because the 1553 interface is not being employed, a third 64 KB SRAM block is freed up for use in this application. System boot would be performed from the on-chip non-volatile C-RAM memory.

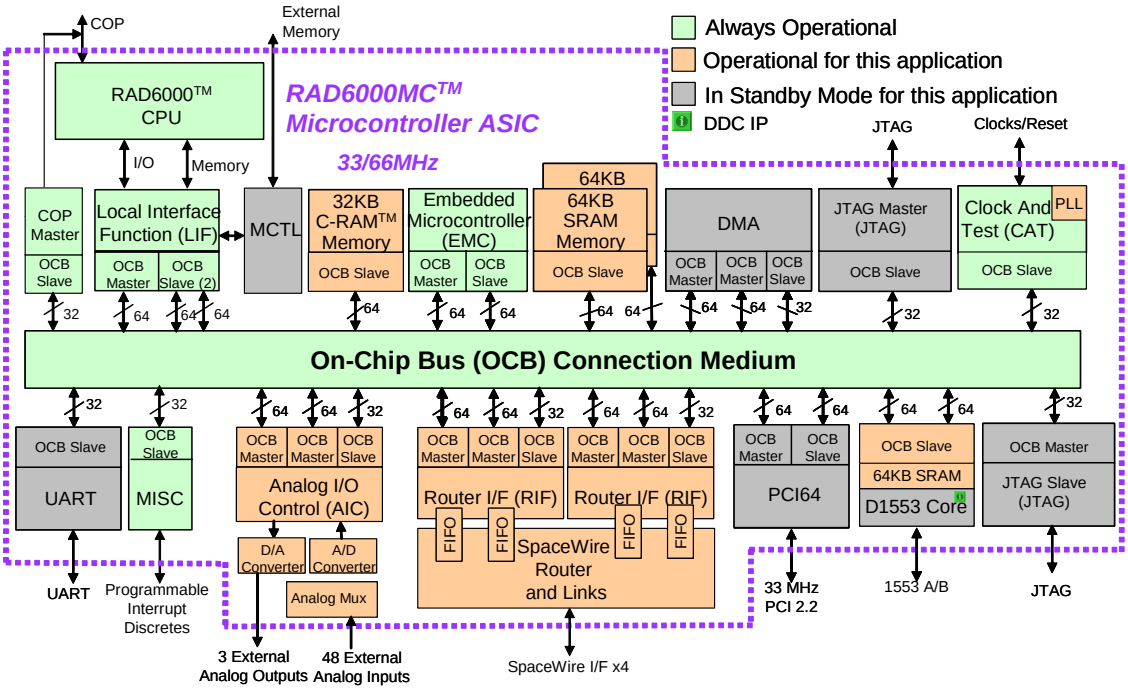


Figure 8: Example RAD6000MC Configuration - Robotic Arm Control

In a minimal configuration running at 33 MHz, the RAD6000MC is expected to dissipate about 2 Watts. With the full configuration operating at 66 MHz, estimated power dissipation is roughly 6 Watts.

SUMMARY

A highly flexible microcontroller ASIC is being designed in a 150nm radiation hardened CMOS technology. It is based on the RAD6000 microprocessor and incorporates a variety of digital and analog cores. Many of the digital cores have already been demonstrated in other ASICs, and the analog circuitry is being manufactured in test chips to provide early hardware validation.

Power and PowerPC are registered trademarks of the IBM Corporation.

RAD6000 and RAD6000MC, and C-RAM are trademarks of BAE SYSTEMS.

Approved for public domain release (VS07-0571) ©2007 BAE Systems All rights reserved

REFERENCES

[1] C.R. Moore, et. al., *"IBM Single Chip RISC Processor (RSC)"*, IEEE 1992 International Conference on Computer Design, pp. 200-204

[2] N. Haddad, et. al., *"Radiation Hardened COTS-based 32-bit Microprocessor"*, GOMAC 1998 Digest of Papers and Journal of Radiation Effects Research and Engineering, Vol. 17, Number 1, April 1999.

[3] J. Marshall, et al, *"Application of Reusable Cores to System-on-a-Chip"*, 2001 Government Microcircuits Applications Conference (GOMAC), March 2001

[4] R. Berger, et. al., *"A Radiation Hardened SpaceWire ASIC and Roadmap"*, 9th Military and Aerospace Programmable Logic Devices (MAPLD) International Conference 2006, September 26-28, 2006

[5] R. Ramaswamy, et. al., *"Progress on Design and Demonstration of the 4 Mb Chalcogenide-based Random Access Memory"*, Proceedings of the 2004 Non-Volatile Memory Technology Symposium, November 2004

[6] J. Marshall, and J. Robertson, *"An Embedded Microcontroller for Spacecraft Applications"*, IEEE Aerospace Conference 2006, March 2006

Approved for public domain release (VS07-0571) ©2007 BAE Systems All rights reserved