SPACEWIRE ROUTER ASIC

Session: SpaceWire Components

Short Paper

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ABSTRACT

A SpaceWire routing switch [1],[2] comprises a number of SpaceWire link interfaces and a routing matrix. The routing matrix enables packets arriving at one link interface to be sent out of another link interface on the routing switch depending on address information at the start of each packet. Thus, SpaceWire packets from one node can be routed, through the switch, to any other node connected to the routing switch.

This paper describes the SpW-10X SpaceWire Routing Switch ASIC designed by University of Dundee and Austrian Aerospace, validated by EADS Astrium GmbH and manufactured by Atmel.

SPW-10X ARCHITECTURE

The architecture of the SpW-10X SpaceWire Routing Switch is illustrated in Figure 1. It has the following main features:

- Eight SpaceWire ports.
- Two external parallel ports, each comprising an input FIFO and an output FIFO.
- A non-blocking crossbar switch connecting any input port to any output port.
- An internal configuration port accessible via the crossbar switch from the external parallel port or the SpaceWire ports.
- A routing table accessible via the configuration port which holds the logical address to output port mapping.
- Control logic to control the operation of the switch, performing arbitration and group adaptive routing.
- Control registers than can be written and read by the configuration port and which hold control information e.g. link operating speed.
- An external time-code interface comprising tick_in, tick_out and current tick count value.

- Watchdog timers on all ports.
- Internal status/error registers accessible via the configuration port using the RMAP protocol [2].
- External status/error signals.
- Implemented in 0.35um MH1RT technology from ATMEL (latch-up immunity guaranteed up to 80 MeV/mg/cm2).
- Prototypes will be in a 196 pin Metric Quad Flat Package (MQFP) whereas the flight models should be in a Ceramic package.

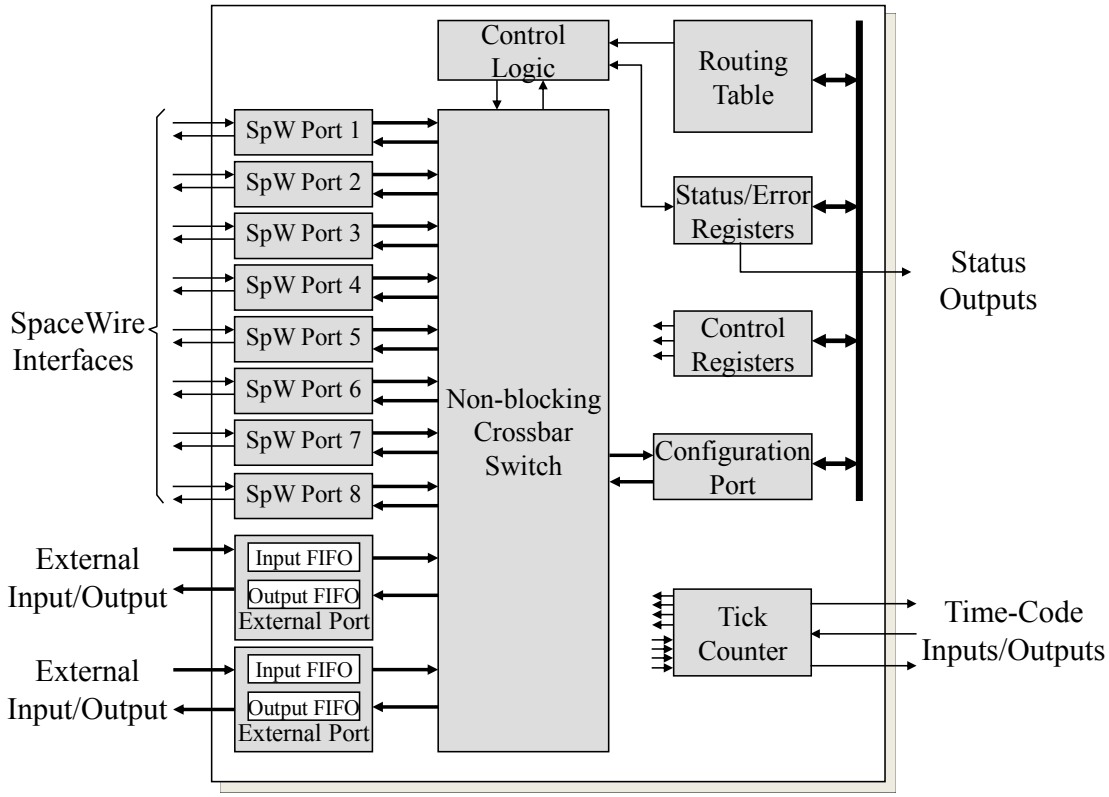

Figure 1 SpW-10X SpaceWire Routing Switch Architecture

SPW-10X DEVELOPMENT AND TESTING

The SpW-10X IP was designed by University of Dundee. Austrian Aerospace prepared this design for implementation in an Atmel radiation tolerant ASIC, EADS Astrium GmbH validated the design and Atmel implemented the ASIC. Funding and overall management was provided by ESA.

The SpW-10X device has been tested in several different ways:

- During design by University of Dundee a VHDL tests bench was used for initial testing. The architecture of this test bench is shown in Figure 2.

- An independent test bench was developed by Austrian Aerospace providing extensive tests and identifying several issues with the initial VHDL code.

- The Router IP was implemented in several STAR-Dundee devices [3] and has been widely used by many organisations.

- The SpW-10X device was implemented in a Xilinx FPGA with the design kept as close as possible to the final VHDL code used for the ASIC design. This SpW-10X FPGA was extensively tested by EADS Astrium GmbH (see Figure 3).

- A second SpW-10X FPGA device was implemented as a mezzanine board in preparation for final ASIC prototype testing (see Figure 4). A similar board has been designed to carry the SpW-10X ASIC.

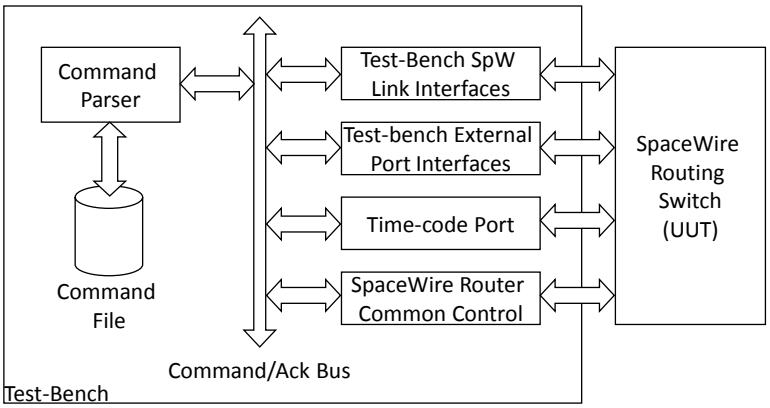

Figure 2 VHDL Test Bench

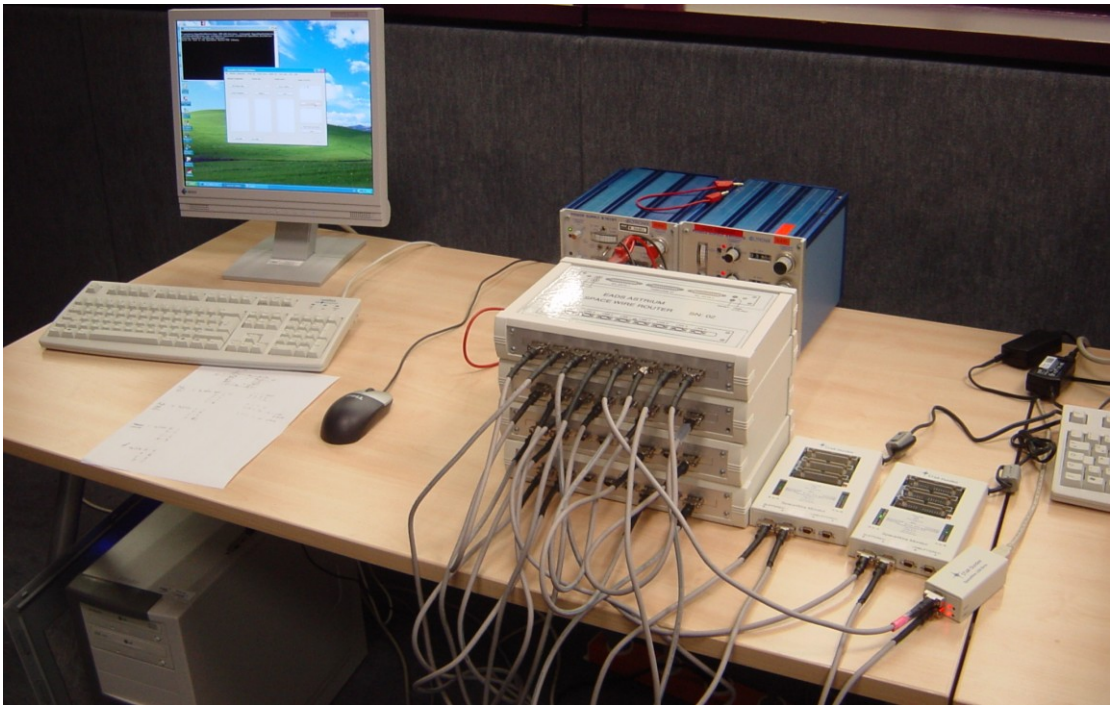

Figure 3 Four SpW-10X FPGA Prototypes Under Test

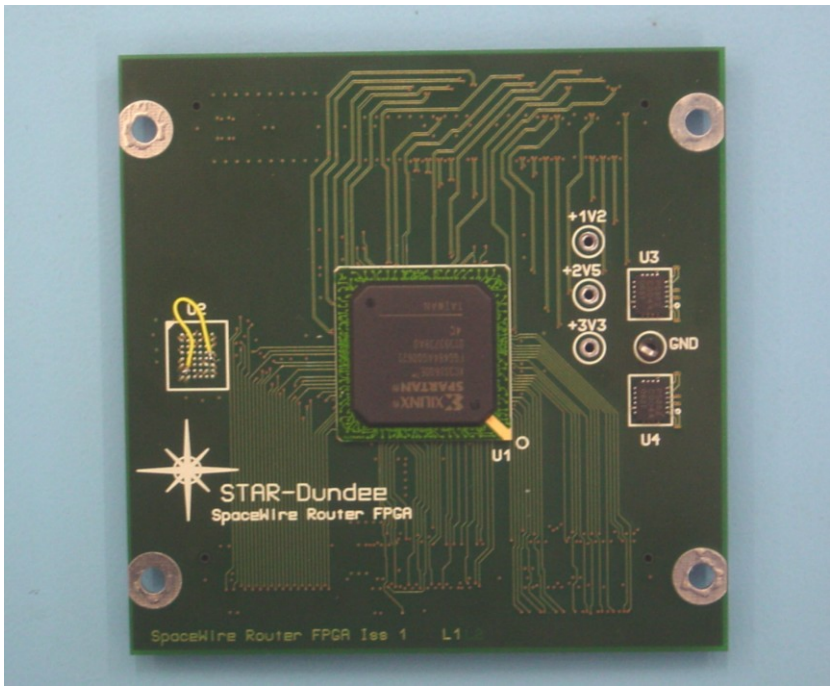

Figure 4 SpW-10X FPGA Mezzanine Board

The prototype ASIC devices are currently being manufactured and are expected in November. A test campaign will then start to characterise the devices. Production devices are anticipated in 1Q08 and will be available from Atmel as the AT7910E. Support for the device will be provided by STAR-Dundee Ltd [4].

SpW-10X Performance

The interfaces on the SpW-10X ASIC are designed to operate at up to 200 Mbits/s. Packet switching times are approximately 0.5 microseconds. Other performance parameters for data character and time-code transmission are detailed in the following tables:

Description	Value	Units
Router Latency – SpaceWire to SpaceWire port	547	ns, max
Router Latency – SpaceWire to External port	317	ns, max
Router Latency – External to SpaceWire port	364	ns, max
Router Latency – External to External port	167	ns, max

Table 1 SpaceWire Router Latency (200Mbit/s example)

Description	Value	Units
Time-code Latency – SpaceWire to SpaceWire port	410	ns, max
Time-code Latency – SpaceWire to External port	317	ns, max
Time-code Latency – External to SpaceWire port	360	ns, max
Time-code Jitter	117	ns, max

Table 2 SpaceWire Router Time-code Latency and Jitter (200Mbit/s example)

These performance values are preliminary and derived either from simulation and/or measurements on the FPGA version.

CONCLUSIONS

A SpaceWire routing switch is a key component in a SpaceWire network. The SpW-10X ASIC has been specifically designed for use in spacecraft onboard data-handling systems. Extensive testing was done on the design prior to manufacture. Prototype devices will be available for further testing and characterisation in November 2007. Following this test campaign they should be available as an ASSP.

ACKNOWLEDGEMENTS

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