

# OVERVIEW OF THE INTA $\mu$ SAT'S DATA ARCHITECTURE BASED ON SPACEWIRE

**Session: SpaceWire missions and applications**

**Short Paper**

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## ABSTRACT

This paper presents the INTA $\mu$ SAT programme initiative and its data bus architecture, which will be based on SpaceWire for high data rate transfers. The first INTA $\mu$ SAT-1 will be an Earth observation mission. This enlarged  $\mu$ SAT class is a further step after the NANOSAT programme success.

Inside the INTA $\mu$ SAT-1 spacecraft, two types of data buses are foreseen. The OBDH data bus will be based on the CAN standard, and it will be a low data rate bus mainly used for TM/TC. In the other hand, it is foreseen a Payload Processor Unit (PPU) with SpaceWire interface for high data rate information exchange, with the cameras and the Mass Memory Unit.

## 1 INTA $\mu$ SAT PROGRAMME INITIATIVE

After successful missions INTASAT (1974) and MINISAT-01 (1997), at the present time, INTA is focusing its efforts on small satellites, with NANOSAT & INTA $\mu$ SAT programmes [1][2]. Most of the subsystems are developed at INTA with bilateral work with research institutions. At the same time, INTA tries to offer parts of HW or SW to the small business Spanish industries, to promote and encourage their entry to the space technology.

The launch of the first Nanosat-01 mission was performed on December 10th, 2004 by an Ariane-5 ASAP from Kourou. Nanosat-01B and it is still working healthy after almost 3 years in orbit, with the same store & forward communication mission and an enhanced UHF antenna, pointed to Earth, is planned to be launched in Oct. 2008 with a Dnepr from Yasny-Rusia. Just as a logical further step to the original Nanosat initiative, in October 2005, INTA started the INTA $\mu$ SAT programme Phase-A feasibility study, to take full advantage of the Ariane-5 launch using ASAP. At present the preliminary design Phase-B is nearing the end (Dec. 2008).

INTA $\mu$ SAT is conceived as a multimission system optimised for 600-700 Km LEO orbits, with inclinations ranging from 0° to 100°. The satellite design is modular with a neat physical separation between the Service Module (SVM) and Payload Module (PLM), that will make easy the design and integration phases for different payloads

(P/L) in parallel with the SVM. The subsystems (S/S) design philosophy is also modular to allow specific resources to be matched to each particular mission, most probably with different flight configurations.

For the first flight it has been selected an Earth observation mission, relying on previous experience with the following cameras at INTA: IRIS, OMC for Integral (2001), and OSIRIS NAC & WAC contributions for ESA mission Rosetta (Jan. 2004). Other astrophysics research payload and GPS signal reflectometry missions will follow. The Control Centre will be installed at INTA in Torrejón-Madrid (same for Minisat-01 and Nanosat-01). The launching date is foreseen for year 2010.

## 2 SYSTEM DESCRIPTION

The basic block diagram is shown in figure 1.

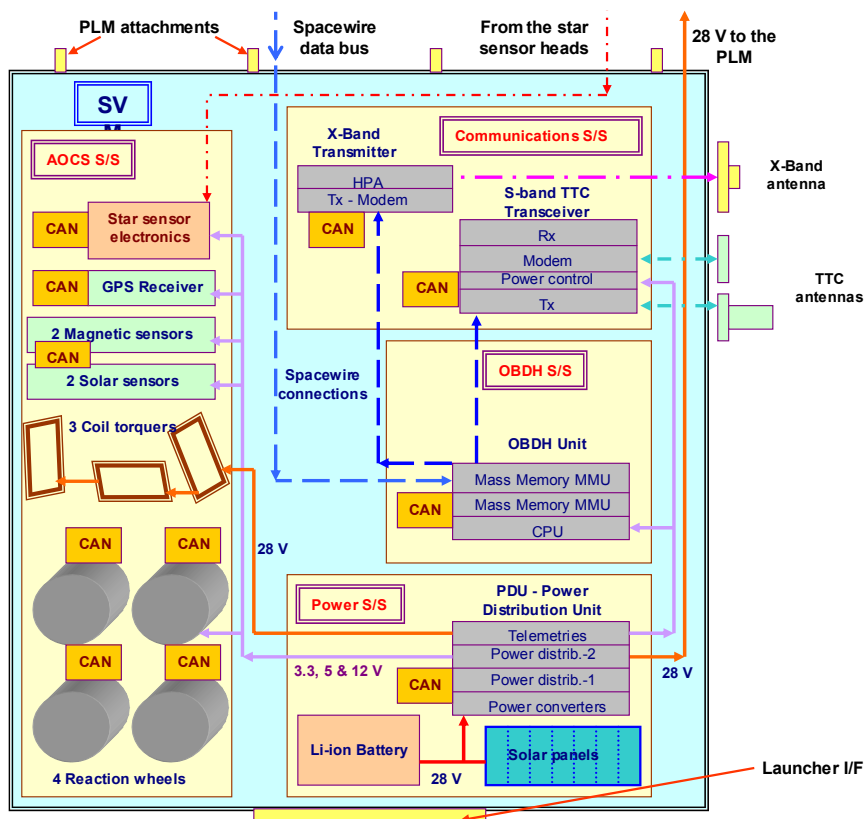


Figure 1. INTA $\mu$ SAT's block diagram

Five subsystems can be identified:

- Structure and thermal subsystem. The structure design is based on a traditional concept with separated SVM and PLM, using a mix of alleviated aluminium plates for the primary structure and honeycomb panels for the secondary one and also the solar panels (in this case with carbon fibre skins). Thermal control is based on the classical passive design, using when required multilayer thermal isolations in the external sides, and radiators where required.
- Communications. This subsystem provides a S-Band channel for TM/TC (up to 2 Mbps) and a X-Band channel for high rate data download (20 to 40 Mbps). It

is based on a digital modem implemented in Actel RTAX-2000 FPGAs, mainly developed by AD Telecom in Barcelona. All the satellite antennas are developed at INTA, where we have long time experience and nice testing facilities.

- Attitude and Orbit Control subsystem (AOCS). An Earth pointing three axis stabilised concept with fast slewing capacity will be used, with A three axes magnetic sensors design for coarse pointing. It has dedicated electronics and a common CAN I/F with the CPU. Additionally, a Star Tracker and a new development Control Moment Gyro (CMG) also called Advanced Gyroscopic Actuator (AGA-150 patented in Spain) will be on board. The CMG will allow fast slewing manoeuvres up to 3°/s in a bang-bang mode.
- On Board Data Handling (OBDH). The OBDH is crucial for the mission success once in orbit and should provide the best performances available today for this kind of small satellites. The Central Processing Unit (CPU) uses Atmel microprocessor TSC-695 (ERC-32), that is a good compromise between performances and full space qualification (Radhard). This is critical, as the design is not redundant. The OBDH subsystem also comprises dedicated Remote Terminal Units (RTU) and a Mass Memory Unit, as it will be explained in section 3.
- Power Distribution Unit (PDU). The primary bus power provided by the 4 fixed solar panels will be a 28 V partially regulated bus concept (battery voltage tracker). The number of strings connected to this bus in real time will be in accordance with the required power in the satellite. The PDU will be responsible for this regulation and for the distribution of secondary regulated voltages (3.3,  $\pm 5$  and  $\pm 12$  V, etc.) to the SVM units that could need them.

### **3 DATA BUS ARCHITECTURE OVERVIEW**

Two data buses can be found inside the spacecraft. The main OBDH bus is based on CANBus standard. This bus is used for low data rate transfers (<500 kbps) such as housekeeping, telecommand distribution, and for ACS sensors & actuators communications in real time with the CPU. CAN protocol provides a low cost and a high reliable bus which has proven suitable for small satellites.

For high data rates, SpaceWire standard has been selected. SpaceWire specification perfectly fulfils the requirements for INTA $\mu$ SAT in terms of speed, reliability, cost and connectivity. SpaceWire will also place INTA $\mu$ SAT in the same direction that ESA is sponsoring, being equipped with the latest technology in intra-satellite communications. Although this decision is challenging, due to its recent and still in development technology, SpaceWire is a guarantee of future.

As shown in figure 2, all subsystems are connected to the CAN bus. For those systems which do not have a CAN interface, a Remote Terminal Unit is provided fully functional to that particular user. The RTU is a System On Chip (SoC) design based on a 80C32 microcontroller. Apart from CAN, the RTU provides different I/O capabilities in order to fit the interface requirements for the most common low and middle range applications.

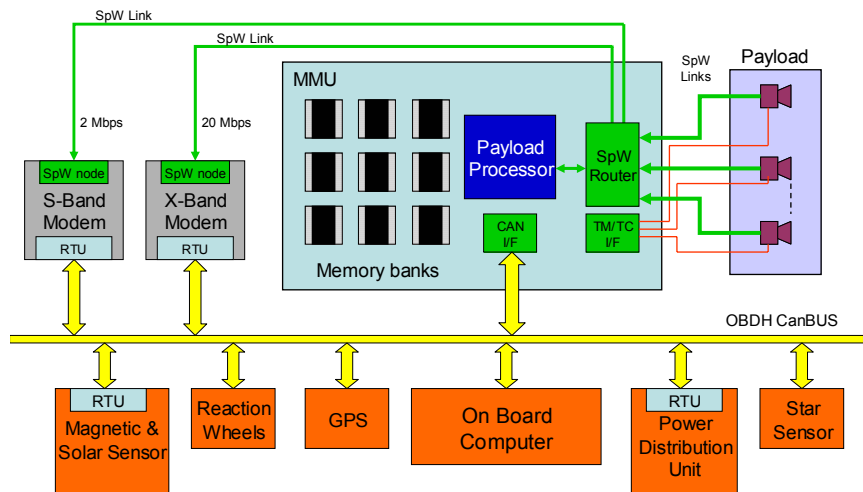


Figure 2. Data bus architecture

The MMU consists of a set of SDRAM memory banks and a Payload Processor as part of a SoC design. Together with the processor, the SoC will provide a SpW router, a low data rate interface with the payload and a CAN interface. The payload processor will handle and pre-process the payload telemetry. During the periods when there is no ground contact, the telemetry will be stored in memory. Otherwise, the stored data is driven to the S or X-band modem for its download to ground in realtime. Both modems are seen as SpW nodes in the SpW network. In the uplink, the S-Band modem sends out the TTC received information to the OBDH-CPU through the CAN Bus. When performing the downlink to ground, the data is taken either from the CPU RAM or the MMU, because both hold recorded data (Housekeeping or payload TM).

#### 4 CONCLUSIONS

INTA $\mu$ SAT-1 development is carrying out according to the foreseen schedule. Thanks to the R+D technology effort dedicated to new developments, INTA expect to have the first mission ready by year 2010. After the first evaluations, SpaceWire has shown as a good design decision, not only in performance, but also as strategic issue. SpaceWire together with other latest technologies will turn Microsat into an up-to date small satellite.

#### 5 ACKNOWLEDGEMENTS

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