# SPACEWIRE FOR OPERATIONALLY RESPONSIVE SPACE AS PART OF TACSAT-4

## Session: SpaceWire missions and applications

## Short Paper

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## ABSTRACT

The rapid integration, launch, and deployment of satellites in response to emerging needs have been a focus of various organizations. This concept has been termed "Operationally Responsive Space" (ORS) by the United States Department of Defense (USDOD). One vision of ORS calls for the positioning in a depot of interchangeable satellite payloads and spacecraft buses with a common interface. Upon direction to deploy a particular mission, the appropriate payload would be selected and integrated with a bus, and the space vehicle would be launched. To support such a system, standardized hardware and software interfaces are needed between the payload and bus. For the development of ORS Bus Standards, the SpaceWire standard (ECSS-E-50-12A) has been specified as part of such a payload-bus interface for high rate data. Data interfaces can be modelled in a number of ways, such as with the OSI layer model. SpaceWire offers the appeal of standardization of physical, data, and network layers. The TacSat-4 satellite, part of the USDOD TacSat experiment series, is intended as a combination of a prototype Standardized Bus for small satellite national security missions and an example payload. This implementation includes an instance of the SpaceWire interface called out in the ORS Payload Developer's Guide. For the bus and payload SpaceWire interfaces, existing SpaceWire logic designs were used, notably the gate array core developed by NASA GSFC. This was intended as a demonstration for ORS that use of existing and freely available intellectual property can streamline design, enhance reliability, and empower instrument and payload vendors.

## INTRODUCTION

Cost and schedule overruns of high-profile satellite systems in the United States [Powner et al, 2006] have led to an increased focus on the development of meaningful capabilities that are achievable relatively inexpensively and on shorter timeframes. Additionally, it is highly desirable to have the capability to deploy space assets rapidly, both in the sense of reducing the duration between call-up and launch, and in minimizing the time it takes to field new technology in orbit. Changes in international relations and the less predictable nature of threats to national and global security that have arisen in recent decades favor space assets that can be launched and utilized quickly.

In pursuing the development of an Operationally Responsive Space (ORS) system, the US Department of Defense has undertaken a multi-phase effort to establish the feasibility, requirements, architecture, and standards involved with such a system. Partnerships between industry, academia, government and research laboratories, and national and international standards organizations have been forged in an attempt to maximize the likelihood of success of the effort. Phase one, led by the Massachusetts Institute of Technology's Lincoln Laboratory, identified and analyzed the missions suitable for an ORS approach and the necessary spacecraft bus and payload capabilities [Brenizer et al, 2005].

Phase two, led by the US Air Force Research Laboratory (AFRL), has focused on ORS technology and device interface standards development. The level of modularity targeted has been at the level of individual spacecraft components, allowing for essentially unlimited combinations of hardware devices for possible satellite configurations. Capabilities have been demonstrated with AFRL's test bed and some will be employed by TacSat-3, due for launch in late 2007. One of these technologies is SPA-S (Space Plug & play Avionics – SpaceWire) [Lyke et al, 2005]. A related AFRL effort, PnPSat, is pursuing the implementation of a satellite using solely plug-and-play components [Fronterhouse et al, 2007].

The third phase has delved deeper into the development of standards to support modularity at a larger granularity. Rather than making every satellite component modular, the space vehicle is split into only two components: the spacecraft bus and the payload. One or two different types of spacecraft buses could support the variety of a dozen or so different payloads identified in the phase one report's collection of missions appropriate for national security space using space vehicles of less than 500 kg [Brenizer et al, 2005]. It is accepted as a cost of ORS that using modular components incurs mass and other over-design penalties that are not present in tailored implementations. To assure the palatability of the resulting standards to industry, about ten companies that might be likely to build the spacecraft buses in accordance with the ORS Bus Standards [ORSBS-002, 2007] in response to a quantity buy request for proposal (RFP) were engaged early in the process by means of the Integrated Systems Engineering Team (ISET). The same group of industry and government representatives on the ISET also developed the ORS Payload Developer's Guide [ORSBS-003, 2007], intended for providers of payloads for ORS missions, and a Launch Interface Standards document [ORSBS-004, 2007].

One area that received considerable attention was that of the spacecraft bus and payload interface. Because the intention was to make the payloads interchangeable, this interface needed to accommodate a wide range of differing applications, corresponding to the phase one national security missions. The concept of operations outlines the existence of a launch depot, where launchers, spacecraft buses, and payloads are stockpiled. Upon call-up, a given payload is mated to a spacecraft bus, forming the space vehicle, and the space vehicle is integrated with the launcher for launch, the whole process perhaps being shorter than several days. Because of the multitude of digital interfaces available for space, a trade study was initiated to determine the best choice for the ORS Standards.

## INTERFACE TRADE STUDY

The digital interface trade study [Jaffe 2006] dealt both with "high speed" and "low speed" interface options, in keeping with a division of electrical interfaces laid out by AFRL in phase two. These divisions were: power and ground, high speed data, low speed data, and time synchronization [Lyke et al, 2005]. For the purposes of the trade study, the boundary between "high" and "low" rate interfaces was considered to be 10 Mbit/s for mission data, excluding any overhead. Though SpaceWire could technically fall into both categories, it was considered as a "high" rate option in the trade study because of its ability to be run at speeds in the hundreds of Mbits/s. It also includes an inherent time synchronization capability with time codes that fulfils an additional interface need. Conceivably, a sufficiently easy-to-implement interface could obviate the need for a "low" rate interface.

To narrow the field of high rate interfaces under consideration, the criteria of supporting rates of at least 50 Mbits/s and of having had at least some spaceflight development heritage were applied. This left the following interfaces and their variants: IEEE-1394 (Firewire), SpaceWire, and Ethernet. Other trade studies have observed the relatively limited spaceflight heritage of Firewire and Ethernet [Walrod, Greeley 2003] [Stakem 2001] [Gwaltney, Briscoe 2006]. These particular three interfaces have been the subject of a considerable amount of comparative research [Walker 2004] [Rakow 2004] [Wolfram 2004] and developmental efforts [Wolfram 2004] [Joseph 2003] [Ivancic et al, 2005] as interfaces for space.

Because there is a dearth of direct empirical comparisons between the interfaces investigated, particularly pertaining to performance and power measures under similar circumstances, it was necessary in some cases to make partially subjective judgments or extrapolate approximations based on the available data. Different implementations also will yield varying figures for some of the qualities measured; the case judged most common was used as the baseline in these situations. The result is more of a meta-analysis than a true trade study, and it certainly not a substitute for actual lab testing.

Many factors can affect speed, throughput, and packet overhead. It may be difficult or impossible to determine optimal or actual performance without lab testing using different schemes and data types. Without controlling for various factors, comparisons may be misleading or invalid. Some such factors include: number of nodes, protocols used, the nature of the data, the desired error tolerance, latency requirements, and compressibility.

A summary of the results of the trade study are seen in Table 1. Shaded boxes indicate that for that particular metric, the interface compares favorably to the other interfaces.

*Table 1. High rate data interface metrics*

| | Firewire | SpaceWire | Ethernet |
|---|---|---|---|
| Speed (Mbps) | 100, 200, 400 | 2 through 600 | 10,100,1000 |
| Packet Overhead | Medium | Low | Medium |
| Standard Maturity | High | Medium | High |
| Radiation Tolerance (TID/SEE) | High | High | Being tested |
| Space Heritage | Low | Medium | Low |
| Rad Tolerant Flight HW Availability | Possibly soon | Yes | >6 months |
| Ground Equipment Availability | Yes | Yes | Yes |
| Flexibility / Expandability | Medium | High | High |
| Power @ 50Mbps loading | ~3W | ~1W | ~2W |
| Mass per node | Low | Low | Low |
| Complexity | High | Medium | High |
| Estimated monetary cost | Medium? | Medium | No basis |

At the time of the conclusion of this trade study in January of 2006, SpaceWire appeared to be the most palatable choice for the high rate interface for the ORS Bus Standards. Ethernet was also attractive, but sufficiently radiation tolerant hardware to meet ORS requirements was not available at the time. (>30Krads total ionizing dose, 60MeV/(mg/cm2) linear energy threshold) It is possible in the future that this will change, and it will be worth revisiting the ORS standards periodically to determine if an update that includes Ethernet is warranted. Firewire had its appeal as well, but it would have been imprudent to select it for the standard before it had been demonstrated in flight. This may also be an interface worthy of revisiting in the future.

Practical considerations for the ORS phase three Standard Bus prototype to implemented for TacSat-4 dictated that the hardware be immediately available. The short schedule did not allow the selection of interface hardware that was not readily available. Relying on the development or future availability of new, unproven flight hardware was an unacceptable option. Additionally, NRL had used SpaceWire with STEREO; and both hardware and field programmable gate array (FPGA) designs were readily available. Ethernet for space, suitable for our orbit, (700 km x 12,050 km inclined 63.4 degrees) was not available. COTS Ethernet components are used for TacSat-1, but they were not appropriate for our HEO orbit. The availability of the 1394 chips used by NPOESS was not assured due to lack of stock and the need for a large order to compel fabrication; an option we could not pursue due to budgetary constraints. The development of the NPOESS 1394 chips (3 per node: APHY, DPHY, and Link [14]) took several years, more than three times as long as expected, and cost many millions of dollars. They are not flight proven as of this writing.

Software layer standards are a critical portion of the interface, but were largely beyond the scope of this trade study. Other efforts are striving to tackle this formidable challenge [McGuirk et al, 2007]

## TACSAT-4 IMPLEMENTATION

The TacSat-4 SpaceWire link has two nodes: The Payload Data Handler (PDH) on the spacecraft bus side, and the Universal Interface Electronics (UIE) on the payload side. They are connected by a nonstandard SpaceWire cable to facilitate ease of rapid depot integration of the bus and payload [Schierlmann, Jaffe 2007]. CCSDS Space Packets and other CCSDS formats are used on top of SpaceWire.

### *Payload Data Handler*

Beyond the payload SpaceWire connection to the UIE, the PDH also provides a second SpaceWire port for ground support equipment or a theoretical future wideband tactical downlink. In addition, it supplies the low rate interface to the payload, a 512 MB solid state data recorder and an eight channel CCSDS Channel Access Data Unit (CADU) multiplex function for the mission data S-Band downlink. Data packet routing is accommodated by a multi-channel chaining DMA controller supervised by the host processor and a Look-Up Table (LUT) that uses the packet destination identification byte to select the appropriate DMA channel for gathering the incoming packets into the required memory partition. The SpaceWire interface was implemented using the SpaceWire VHDL FPGA core developed by NASA's Goddard Spaceflight Center. This core is now widely available for

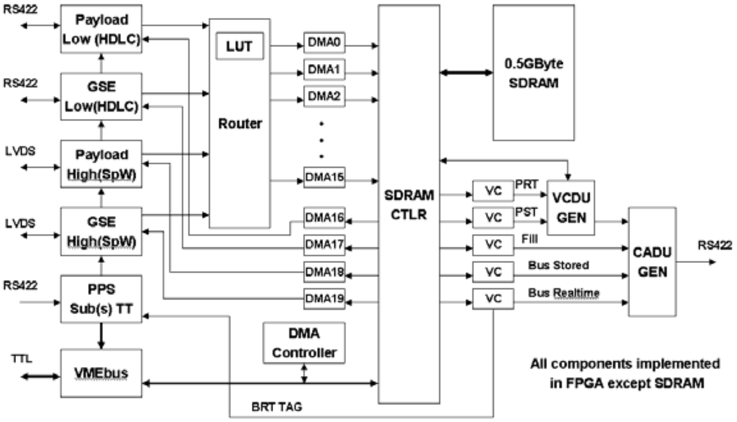

*Figure 1. PDH block diagram*

many users for no monetary cost. Digital logic was implemented in an Actel RTAX2000 FPGA utilizing the onboard RAM memories configured in Triple Module Redundancy (TMR) to mitigate Single Event Upset (SEI) effects. One of us (Greg Clifford) was the design engineer for the PDH.

### *Universal Interface Electronics*

The UIE is intended as a versatile compact avionics system. Its different interfaces allow it to easily perform as a protocol translator. Depending on the desired configuration, it can have up to six SpaceWire ports. It can also offer several RS-422 ports, analog and digital I/O, power switching, and data storage. It employs the LEON3 processor in an Actel RTAX2000 FPGA and also includes a Xilinx Virtex II FPGA for mission-specific configurations. Both Goddard and Gaisler SpaceWire cores are utilized in the UIE. One of us (Jeff Summers) is the project manager for the UIE.

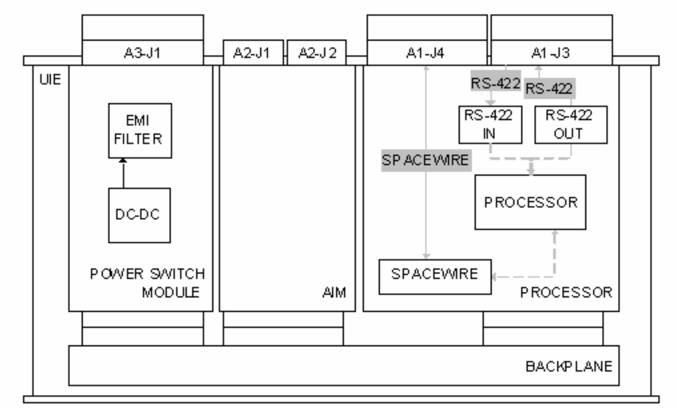

*Figure 2. UIE block diagram*

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