A SpaceWire Implementation of Chainless Boundary Scan Architecture for Embedded Testing

Session: SpaceWire onboard equipment and software embedded

Short Paper

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Abstract

Electronic equipment for complex digital payloads have become increasingly more sophisticated incorporating thousands of ASICs with intensive interconnect between them. Most of these ASICs have to be monitored and controlled to satisfy the mission operational requirements. One scheme for implementing this is by connecting all these ASICs using a reliable network and interconnect such as SpaceWire. The ASIC in the system act as nodes which include their own SpaceWire routers. The testing and validation of the all electrical interconnects in such a complex system becomes a major contributor to increasing the schedule and cost of a project. Therefore built in self test, embedded test, strategies have been employed to alleviate these issues.

Traditionally IEEE Std 1149.1(JTAG) Boundary scan testing standard has been used to implement embedded test. Components in the system have to be daisy chained and driven by the JTAG control bus in parallel. Such an architecture has a number of limitations: Firstly, a faulty ASIC within a daisy chain will prevent testing of the whole chain. Secondly the parallel JTAG control bus puts undesirable constraints on the design of reliable systems. To overcome these limitations, and make the boundary scan test infrastructure transparent and independent of the design of the system under test, a generic chainless boundary scan architecture has been developed. This architecture is well suited to systems which use SpaceWire networks.

This paper proposes a dual function for the SpaceWire network. One, to facilitate the performance of embedded test. The other, is its standard role in communicating data and commands between nodes. A UK patent [1] application has been filed covering the method, architecture and technology described in this paper.

1. Introduction

The validation of modern complex electronic systems [2] now demand that facilities and features to test the system are incorporated as an integral part of its architecture requiring very little and possible no external test equipment at all. This approach is referred to as embedded test.

Traditionally IEEE Std 1149.1 (Standard Test Access Port and Boundary-Scan Architecture) [3] has been used to implement embedded test. Components in the system have to be daisy chained and driven by the JTAG control bus in parallel. Such architecture has a number of limitations: Firstly, a faulty ASIC within a daisy chain will prevent testing of the whole chain. Secondly the parallel JTAG control bus puts undesirable constraints on the design of reliable systems.

The solution is to develop and incorporate advanced highly integrated embedded test elements which will enable a built-in test infrastructure to evolve simply as by-product of the architectural design of the system it is intended to test. Such an advanced embedded test solution is inherently independent to the architecture configuration of the system it is built-in to test. This proposed embedded test solution is referred to as “Chainless Boundary Scan” and is well suited to systems which use SpaceWire networks as shall be described in this paper.

A typical SpaceWire [4] network is illustrated in Figure 1. In this example, the processors (P1 to P4) in the processor array are directly connected to one another. The sensors, memories and processor array are interconnected via the routers. Redundancy is provided in this example network by the use of redundant links and a pair of routers. If data is being sent from Sensor 1 to Memory 1 via Router 1 and the link between the sensor and the router fails then data can be sent from Sensor 1 to Memory 1 via Router 2. As described earlier, the SpW network interconnecting the components of the system is designed to enable information to be passed around the network even when at least one SpW link or the component itself has failed.

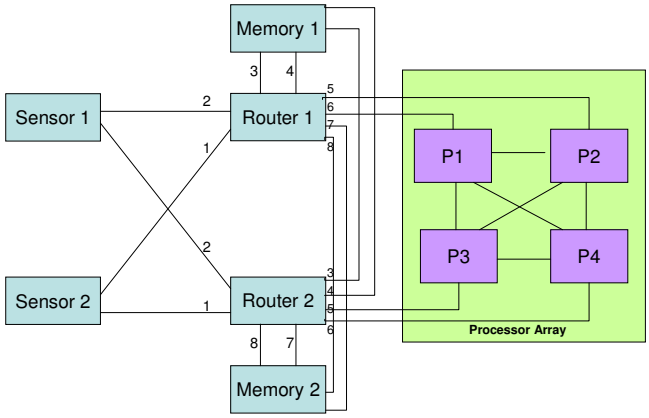

Figure 1: A typical SpaceWire Network

2. Background to Boundary Scan IEEE-1149.1 Standard

IEEE 1149.1 testing standard (also referred to as JTAG standard) is a test architecture which is used for designing boundary-scan test circuitry into digital integrated circuits for the purpose of testing the IC and the interconnections between them when assembled into a system.

All boundary scan compatible devices have a Test Access Port (TAP) with four required pins: Test-Data-Input (TDI), Test-Data-Output (TDO), Test-Mode-Select (TMS) and Test-Clock (TCK). An optional fifth Asynchronous Test-Reset (TRST) may be provided. At a system level, devices to be tested using boundary scan are connected in a chain referred to as a "scan chain". In the chain, the TDO of one device is connected to the TDI of the next device in the chain. The TDI of the first device in the chain is typically connected to the external boundary scan equipment via a "scan port". Similarly the TDO of the last device in the chain is also connected to the "scan port". The other signals listed above are passed through the "scan port" and are connected in parallel to all devices in the "scan chain".

Typically, a module incorporating boundary scan is designed with only a single "scan chain". However, there are instances where buffering requirements, redundancy management, the use of different interface logic (e.g. ECL/TTL) and power supply levels and clock domains on the same board, impose the need for multiple "scan chains", with each chain having its own "scan port". At system integration, modules that require boundary scan tests to be carried out between them must all have their scan ports connected to the same boundary scan test equipment. This is typically implemented using a multi-drop connection scheme.

3. Chainless Boundary Scan Architecture

The proposed 'chainless boundary scan architecture is based on a mesh network topology and allows the system design to be independent and free of the constraints imposed by a traditional daisy chain boundary scan architecture. One way to implement this is by exchanging the boundary information to the components under test via asynchronous communication links. These links can be individually routed or passed via the components under test which shall be referred to as 'nodes'. This strategy/approach would enable the system components themselves to facilitate the implementation of chainless boundary scan architecture as opposed to the traditional approach thus reducing component count and simplifying system design.

A system implementation of the "chainless boundary scan archetectiure" using SpW as the asynchronous communication links to distribute boundary scan information will be described with reference to Figure 2. The system consists of four boundary scan compatible integrated circuit devices C1 to C4 with a number of SpW communications links interconnecting each device with the other devices of the system. Each component may be regarded as a SpW node and incorporates a SpW interface as part of their normal functional requirements.

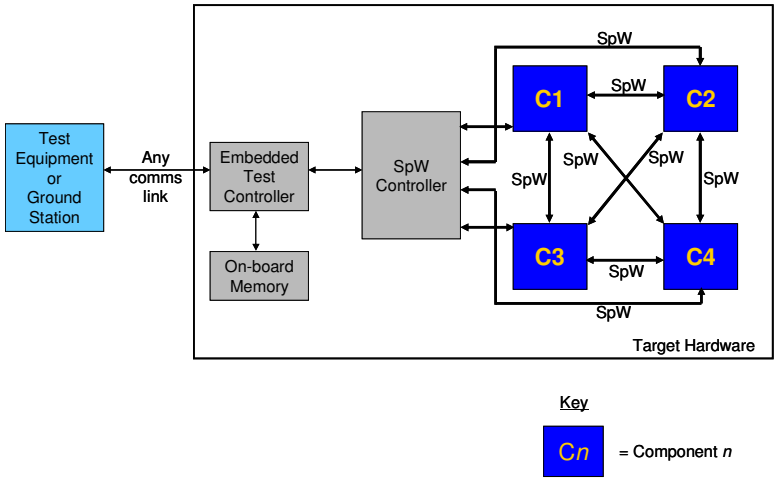

Figure 2: An example embodiment of the Chainless Boundary Scan Architecture

A key feature of the chainless architecture is that there is no requirement that the components to be tested using boundary scan are connected in a "scan chain" with the TDO of one device being connected to the TDI of the next device in the chain.

Instead, the system's SpW network is used to pass the boundary scan information when performing embedded test by using an integrated SpW router to boundary scan adapter IP block shown in Figure 3.

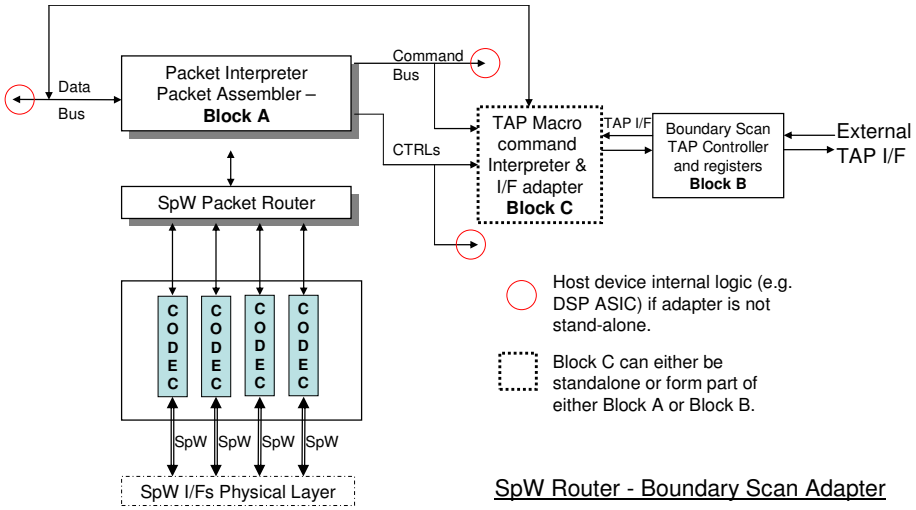

Figure 3: SpW Router to Boundary Scan Adapter

This IP block can be used either stand alone of as an integral part of the system components be it an ASIC, an FPGA or a unit. The basic functions of this IP block are:

- 4 x SpW I/F.
- 4 x Space Wire CODECs
- 1 x SpW Packet Router. The router also interfaces with a parallel interface where data on the Space Wire network can be presented if it was addressed to it.
- Space Wire packet interpreter and assembler block – Block A. This block is responsible for decoding commands arriving on the Space Wire interface and routing or processing the associated data or/and command appropriately. For the chainless boundary scan architecture described in this implementation of the claim it is necessary for this block to connect to the TAP controller block and associated boundary scan data and command registers.
- The Boundary scan TAP controller block – Block B. This block is responsible for generating all the necessary signals to drive the device's boundary scan circuitry and interfaces. This block also has an external Boundary scan TAP interface which would allow it to drive an external boundary scan chain of one or more boundary scan-able devices. The interface between the TAP controller block and the Space Wire packet interpreter and assembler block as designated as block C. The TAP controller would have a specific address or designation so that associated boundary scan commands and data transported on the Space Wire network can be communicated to it by the Space Wire packet Interpreter and assembler block.
- External conventional boundary scan IEEE 1149.1 Test Access Port (TAP) to enable testing of standard boundary scanable components that do not have SpW interfaces.

To perform a boundary scan test on this system, a boundary scan embedded test controller (ETC) as shown in Figure 2 is required to generate IEEE1149.1 boundary scan commands and data as well as receive and analyse scan data from the devices under test. This boundary scan information exchange is performed over SpW links between all the components under test and the boundary scan test controller. The primary function of the ETC is to sequence the tests in an appropriate order and execute the IEEE 1149.1 test vectors for in-orbit level test and diagnosis. To enable embedded and stand-alone boundary scan tests to be carried out, the test sequences are stored in a flash memory block and are accessed via the ETC under the control of the on-board processor. For System level test, at least one ETC is required.

4. Conclusion

This paper has demonstrated the viability of using asynchronous links to implement boundary scan without relying on the traditional daisy chain boundary scan infrastructure.

The advantage of the chainless boundary scan architecture described above, is that boundary scan tests can still be performed even after one or more components have been disabled, configured in functional mode or have failed.

The proposed scheme is advantageous in that it allows boundary scan test vectors to be transported via any appropriate communications link to the target hardware and directly executed on it without having to convert from and to an IEEE1149.1 interface. The method also facilitates communication between components on the target hardware to enable IEEE1149.1 testing without having to use external TAP controller signals.

This reduces the non-recurrent as well as recurrent costs of developing and producing a system. The added benefit is that this type of embedded test solution can be used to test and validate the system throughout its lifecycle, from leaving the assembly line to and including in-orbit testing in any permitted configuration.

5. References

[1] Patent Application Number 0712373.0, Inventors M Ali and O Emam., "Embedded Test System and Method", 2007.

[2] M Ali, O Emam, P Horwood and P Collins, "Implementation of 1149.1 and Scan chip set solution to Test Astrium Communication Space Satellites", International Test Conference (ITC), Baltimore, 2002.

[3] IEEE1149.1a – 1993 Standard, IEEE Standard Test Access Port and Boundary scan Architecture

[4] "SpaceWire – Links, Nodes Routers and Networks", ECSS-E-50-12A, January 2003.