RAD750TM SpaceWire-Enabled Flight Computer for Lunar Reconnaissance Orbiter

Session: SpaceWire Onboard Equipment and Software

Short Paper

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ABSTRACT

An additional version of the RAD750TM CompactPCI[®] 6U radiation hardened single board computer has been developed and delivered for use on the Lunar Reconnaissance Orbiter (LRO) mission developed by NASA Goddard Flight Center, scheduled to launch in late 2008 as the first mission in preparation for manned missions to the Lunar surface. This new variant of the RAD750 processor incorporates both a SpaceWire router and 1553 interface. The LRO mission processor architecture represents a hybrid implementation in which the SpaceWire links, 1553 bus, and PCI bus are all utilized to interconnect the flight computer and on-board instruments. The RAD750 computer includes 36 MB of radiation hardened SRAM, 4 MB of non-volatile memory, and the ability to support PROM or EEPROM in its SUROM locations. The computer also includes an additional 8 MB of radiation hardened SRAM dedicated to supporting the SpaceWire ASIC that provides a four port router through a PCI interface. The 1553 interface consists of an Actel FPGA, Aeroflex "SµMMIT DXE" ASIC, and dedicated memory. SpaceWire transport layer software was developed for the embedded microcontroller that resides on the SpaceWire ASIC using a C compiler developed by BAE Systems.

This paper discusses the definition of the new processor board configuration, definition and development of the software, and validation of the board through delivery to the mission. In addition, a preview of the next generation RAD750 processor board will be discussed, in which an improved four port SpaceWire router is incorporated directly into the third generation Power PCI bridge ASIC. This increased level of integration improves size, weight, and power of the flight computer while also adding features and increasing performance.

LUNAR RECONNAISSANCE ORBITER MISSION AND ARCHITECTURE

Lunar Reconnaissance Orbiter (LRO) is the first mission of NASA's Lunar Precursor Robotic Program (LPRP), supporting the planned return of astronauts to the Lunar surface. Scheduled to launch in October 2008, LRO will orbit the moon for one year in a 50km circular polar orbit [1] scouting possible manned landing sites, with potential extension of the mission for an additional four years. The spacecraft will deliver up to 450 Gigabits of data back to Earth each day. The spacecraft payload includes seven instruments, two of which are connected to the Command and Data Handling (C&DH) unit developed by NASA Goddard Space Flight Center via the SpaceWire network, as shown in Figure 1.



Figure 1: Lunar Reconnaissance Orbiter C&DH / Spacecraft Architecture

The Lunar Reconnaissance Orbiter Camera (LROC) instrument includes three cameras, two narrow angle with 0.5 meter resolution and one wide angle with 100 meter resolution. LROC implements the SpaceWire protocol and physical layer in a Xilinx FPGA. The LROC instrument will supply the majority of information sent back to Earth. The Mini-Radio Frequency (Mini-RF) instrument is a demonstration of S-band and X-band synthetic aperture radar, connected to the SpaceWire network through BAE Systems' SpaceWire ASIC [2]. The remaining instruments interface to the C&DH via the MIL-STD-1553 bus.

Within the C&DH unit, the RAD750 flight computer communicates with the instruments and other boards via three interfaces: a four-port SpaceWire router, a 32bit, 33 MHz PCI bus, and a redundant MIL-STD-1553 bus. The SpaceWire router is implemented in BAE Systems' SpaceWire ASIC that is in turn connected to the RAD750 microprocessor via the PCI bus and the second generation enhanced Power PCI bridge ASIC. Both the Ka-band and S-band communications boards include SpaceWire interfaces with routers, implemented in Actel FPGAs. The LROC instrument is connected directly to one of the processor board's SpaceWire links, while the Mini-RF connects to the Housekeeping and Input/Output (HK/IO) board that also implements a SpaceWire router using an Actel FPGA and is then routed to the processor board across the SpaceWire bus via the FPGA that implements another SpaceWire router. The 400 Gigabit LRO mass memory is implemented in synchronous DRAM that is interfaced to the RAD50 computer via the PCI bus on a custom C&DH backplane.

RAD750 SINGLE BOARD COMPUTER (SBC) ARCHITECTURE

The RAD750 flight computer is a CompactPCI 6U-220 card with two printed wiring boards (PWBs), an extension of the RAD750 CompactPCI 3U single board computer [3] that is currently flying on NASA's Deep Impact and Mars Reconnaissance Orbiter missions. The RAD750 microprocessor [4] operates at 132 MHz with a 66 MHz bus to I/O and memory, both of which are accessed through the enhanced Power PCI bridge ASIC [5]. A total of 36 MB of radiation hardened SRAM is available to the RAD750, along with 4 MB of EEPROM and 64 KB of Start-up ROM, all provided with additional bits for error correction code (ECC). The processor PWB as shown in Figure 2 is not a standard CompactPCI configuration in that there are three on-card PCI loads on the PCI bus that are made visible to the backplane. The enhanced Power PCI bridge ASIC, the SpaceWire ASIC, and the Actel FPGA programmed as a SµMMIT-PCI Interface (SPIF) for access to the 1553 bus all include PCI interfaces based on the same flight-proven reusable core developed by BAE Systems. In addition to the RAD750 microprocessor, the processor PWB includes 20 MB of SRAM memory with ECC, 8 MB of which is dedicated to the SpaceWire ASIC that includes its own external memory controller. The 1553 bus interface consists of the SPIF FPGA, the Aeroflex SµMMIT DXE ASIC, 64 KB of dedicated memory, and transformers. The back-side 160 mm memory MIB includes 24 MB of SRAM and 4MB of EEPROM, all with ECC. Connectors for the four SpaceWire links and the dual redundant 1553 are located on the single board computer's face plate, along with a connector for the RS-422 discretes and a test connector.

The board uses the standard CompactPCI 5 volt and 3.3 volt external power inputs supplied through the backplane. Separate, switchable, 5 volt input pins are provided to power the Local Memory EEPROM devices. The 2.5 volt supply required for the SRAM, ASIC and FPGA cores is generated on the board by International Rectifier linear regulators. Separate Q-Tech oscillators are employed for the main system clock (66 MHz) and the 1553 bus (24 MHz). Eight RS-422 (4 in, 4 out) discrete interfaces are provided. Power dissipation of the RAD750 single board computer has been measured at between 5.5 and 17 Watts in this configuration with calculated typical upper limit of 19.1 Watts. The mass of the RAD750 SBC is 3.5 pounds.



Figure 2: RAD750 Single Board Computer LRO configuration Front Side

SPACEWIRE INTERFACE IMPLEMENTATION ON THE SBC

The SpaceWire ASIC, shown in Figure 3 is based on BAE Systems' reusable core architecture. Its primary function is to perform routing of data using the SpaceWire protocol via a router with four external links and two internal connections to the On Chip Bus, the standard cross-bar switch connection medium of the reusable core architecture. In addition to the SpaceWire links and router, the ASIC is comprised of an external memory controller, dual PCI interfaces, a DMA controller, and cores for clocks and JTAG test support. Two 16 KB blocks of on-chip scratchpad memory are provided, as well as a 32-bit RISC processor called the Embedded Microcontroller (EMC) [5]. The EMC performs housekeeping functions as well as providing support for the SpaceWire router. A Phase Locked Loop (PLL) is provided for the SpaceWire link interface, which is capable of 280 MHz operation.



Figure 3: BAE Systems SpaceWire ASIC

In the LRO implementation, the PLL has been throttled back to only 132 MHz, supporting an aggregate system throughput of 170 Mb/s across the four ports of the SBC's SpaceWire ASIC. The gating link is the 100 Mb/s transmission between the processor and the K-band communications board. Data transmission from the LROC instrument to the processor requires 30 Mb/s throughput across a SpaceWire link. The Mini-RF instrument, which communicates with the processor via a chained SpaceWire connection through the HK/IO board, provides data at a 28.5 Mb/s rate.

SPACEWIRE SOFTWARE SUPPORT

Software drivers have been developed for the SpaceWire ASIC using C code and are included in the RAD750 Board Support Package (BSP). The BSP is designed for operation with the VxWorks (versions 5.4, 5.5, and 6.2) Real Time Operating System (RTOS). The device drivers include modules for the Programmable Interrupt Discretes (PIDs), interrupt routing, PCI and address translation, the DMA controller, the Router Interfaces (RIF) and the configuration of the SpaceWire router. The SpaceWire interface is controlled by a combination of the on-chip EMC core within the SpaceWire ASIC and the RAD750 processor across the PCI bus. The RAD750 control software also includes a network routing layer that resides above the device driver. This network layer provides queues for incoming packets. Code development for the EMC core is supported by a C compiler that BAE Systems has developed expressly for it.

Software support for the Consultive Committee for Space Data Systems (CCSDS) File Delivery Protocol (CDFP) is split between the RAD750 CPU and the EMC within the SpaceWire ASIC. The function of the software executing within the SpaceWire ASIC is to assist in CFDP download to maximize downlink throughput by sending batches of CFDP data packets known as Protocol Data Units (PDU) over the SpaceWire interface to the Ka-band communications link. Code developed for the EMC using its C compiler is used to partition large files for efficient transmission by generating PDU headers and control block "descriptors" on large (1 MB) blocks of file data. The RAD750 processor handles the supporting PDUs required for a CFDP transaction, including Metadata, End of File (EOF) in which a checksum is provided, and positive acknowledgement (ACK) or negative acknowledgement (NAK) in cases where a reliable service version of CFDP is employed.

SPACEWIRE-BASED DATA TRANSFER OPERATIONS

When data is sent to the SpaceWire ASIC on one of the SpaceWire links, it is sent through the router and on to the On Chip Bus. From there, it may either be transferred into the SRAM that is dedicated to the SpaceWire ASIC or across the PCI bus and through the enhanced Power PCI bridge ASIC into the RAD750 microprocessor's memory. A Direct Memory Access (DMA) transfer is then used to move the data into the mass storage file system.

When downlink of this data is desired, the data is extracted from mass memory with another DMA operation issued by the SpaceWire ASIC, is moved across the PCI bus and is stored in the SRAM associated with the SpaceWire ASIC. Supporting PDUs are generated by the RAD750 and the EMC within the SpaceWire ASIC issues DMA chains to packetize the data and send it across the SpaceWire link to the downlink transmitter.

Two sets of DMA engines support the transfer operations. One set of memory-tomemory DMA engines are used to transfer the data between RAD750 memory, SpaceWire memory and Mass Storage memory. A second set of DMA engines are used to transfer data between RAD750 memory or dedicated SpaceWire memory and the SpaceWire link.

INTEGRATION OF THE RAD750 COMPUTER WITH THE LRO SPACECRAFT

The RAD750 single board computer (SBC) has been successfully integrated into the LRO C&DH Engineering Test Unit (ETU). Extensive testing was performed on the single board computers at the box level prior to integration with the full spacecraft. A combination of built-in self-test (BIST) of individual components and functional tests were executed to validate all parts of the board. Functional tests included system stress tests, testing of error correction of the memory, and transfers across the PCI, 1553, and SpaceWire interfaces.

The LRO C&DH ETU has now been integrated into the FlatSat (Flat satellite) test bed at the NASA Goddard Space Flight Center and is performing well. SBC breadboard cards were delivered during 2006. SBC engineering units were delivered early in 2007 and two flight units were delivered to NASA in mid-2007. NASA is currently considering using this SBC configuration in additional missions.

The LRO RAD750 SBC is being used on NASA's Lunar Crater Observation and Sensing Satellite (LCROSS) C&DH. LCROSS is overseen by NASA Ames Research Center and is scheduled for launch in 2008. It will travel to the Moon as a comanifested payload aboard the Saturn 5 Launch Vehicle [6] for the LRO.

NEXT GENERATION SPACEWIRE-ENABLED RAD750 SINGLE BOARD COMPUTER

A RAD750-based single board computer (SBC) is currently in development that increases the level of integration of the SpaceWire interface, as shown in Figure 4 in conceptual form. The next generation of the Power PCI bridge ASIC, designed in 150nm CMOS technology, incorporates both a SpaceWire router with four link interfaces and a dual redundant 1553 interface as internal cores. This will allow the board format to reduce to the more standard 6U-160 format with decreased power dissipation, as the SpaceWire ASIC, the SPIF FPGA, and the Aeroflex S μ MMIT

ASIC with dedicated SRAM memory chips will no longer be required. On-chip memory has been extended to include two 64KB cores in addition to SRAM for the 1553 interface. In the new ASIC, performance of the SpaceWire interface increases to greater than 300 MHz.



Figure 4: Next Generation RAD750 CompactPCI SBC Conceptual View (Front Side)

The RAD750 processor performance has been increased to 200 MHz, and an external 1MB Level 2 cache has been added. System SRAM capacity on the new SBC will also increase to approximately 200 MB, with new 16Mb SRAMs packaged in 80 Mb stacks replacing the current 4Mb chips that are packaged in 20Mb stacks. Startup ROM and any additional non-volatile memory will be implemented with BAE Systems' C-RAMTM memories. Prototype versions of this next generation RAD750 board are expected in 2008, with flight units planned for 2009.

SUMMARY

BAE Systems has developed a SpaceWire-enabled Single Board Computer based on the RAD750 microprocessor. Flight boards have been delivered for use in the Lunar Reconnaissance Orbiter mission, scheduled to launch in late 2008. BAE Systems continues to emphasize the integration of the SpaceWire protocol and plans to offer a next generation SpaceWire-enabled processor board by 2009.

References

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