A METHODOLOGY AND THE TOOL FOR TESTING SPACEWIRE ROUTING SWITCHES

Session: SpaceWire test and verification

Short Paper

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ABSTRACT

SpaceWire routing switches could include functions of multicasting and adaptive routing. But supporting of these functions essentially complicated verification and testing process.

The article presents the developed test shell for verification and parameter evaluation of routing switches with different number of ports and for networks with different topology and number of switches; for data packet flows automatic generation with different parameters. Also the test shell could be used for testing of RTL models and post-synthesis netlists.

We use SystemC and Cadence SimVisio (simulator ncSim) design tools for these test shell development. SystemC provides development of parameterized models with flexible behaviour. SimVisio tools allows integration of mixed language models (SystemC, VHDL, Verilog) in one project.

1 INTRODUCTION

A network model is represented by the parametrized shell that includes models of SpaceWire routing switches, terminal nodes, interconnection lines, and a control and monitoring block. When a user specifies parameters (number of nodes, switches, interconnections topology, and other parameters) the shell configures the network model automatically. We use two network topology specification methods: a universal one – a network is described by a full interconnection graph specification, and a method for regular topologies specification (e.g. different meshes, hypercubes). In the second method a network structure is described analytically; topology type and number of nodes is user defined. The examples of networks are showed on the figure 1.

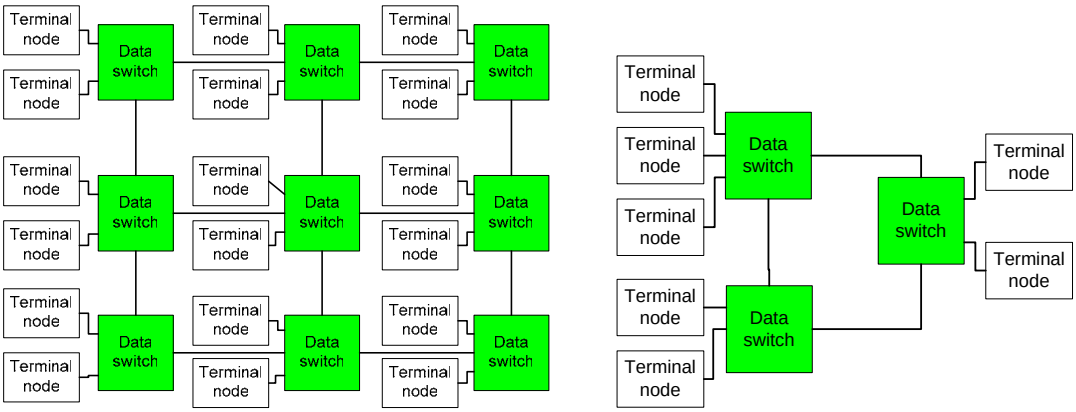

Figure 1. Examples of switch based networks

Users could apply this model for verification and parameter evaluation of his SpaceWire routing switches.

We not present on figure 1 the control and monitoring block. It connected to all terminal nodes and data switches for performing simulation control (initialization of routing switches and terminal nodes, starts data transmission, global result checking). The models of the shell, routing switches, terminal nodes, interconnection lines, and a control and monitoring block are written in SystemC. RTL routing switches models on VHDL or Verilog and netlists (VHDL, Verilog) also could be used.

The included into the network components could be described with different detalization. This allowed us choose between the resultant accuracy and reasonable simulation time. We develop some switch models on systemC with different detalization for preliminary simulation and parameter evaluation. We are using these models for selection bufferisation method and buffer size, for selection and verification arbitration scheme, and for decision some other questions affect to switch performance. The network models, included RTL models of data switches or netlists, are more detailed. The structure of these models illustrated by figure 2

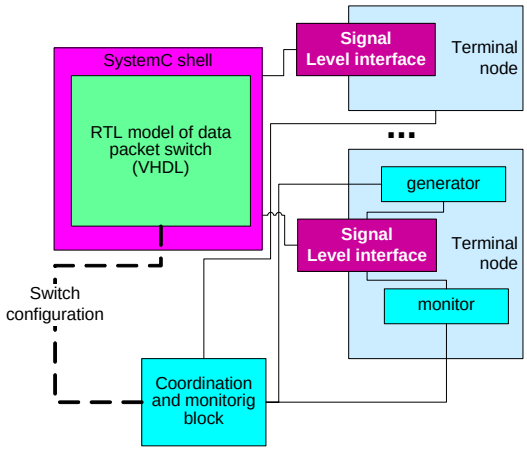

Figure 2. Example of network model included RTL model of data switch

These models includes some special components: SystemC shells for components described on VHDL and Verilog (these shells required by Cadence design tools) and

signal level interfaces for terminal nodes (basically terminal nodes have not signal but character level interfaces)

The models, suggested in this article, are correlated with SpWFM model created in SUAI, but oriented to detailed simulation of different arbitration schemes and to test and verification of RTL and netlists switch descriptions.

2 VERIFICATION AND TESTING PROCESS

The test process in our model includes next three stages:

1. The initial configuration stage. On this stage the coordination and monitoring block executes initial settings for switch models and terminal nodes models. Initial settings for switch models includes writing information for logical addresses to routing table, writing appropriate values to adaptive group registers and if RTL models of switches are used writing appropriate values to implementation specific registers. Initial settings for terminal nodes include data flow and control codes flow parameters.

2. The data packet transmission stage. On these stage data packets are transmitted between the switches and the terminal nodes. The duration of this stage could be assigned as absolute value or user could assign number of packets that are transmitted from every terminal node. The terminal nodes execute preliminary control of data packet transmission and timing parameters evaluation at this stage.

3. The global data packet control and collects statistics.

During data packet transmission testing we need to control: packet header must be excluded from the packet or not excluded according routing table settings; packet contents and end-of-packet symbol must follow without changes. The set of ports, which received this packet, must correspond to its address and adaptive routing settings. For transmission control every packet contents includes special information. The packet generator writes every transmitted packet into a log file. When the monitor receives the packet it uses log files for control packet contents and end-of-packet symbol, control of packet header processing. But only the coordination and monitoring block executes final packet header processing control. It controls multicast transmission and adaptive group routing. It control that multicast packet received by all terminal nodes includes in appropriate multicast group and not received by any other terminal nodes. Also it check that packet addressed to terminal node includes into adaptive routing group (or translated via switches which ports includes in adaptive routing group) is received by only one terminal node from appropriate adaptive routing group. The and monitoring block used adaptive routing registers values, routing tables ad special information includes into packets. This special information includes number of source terminal node, address field (for some addressing types address field is deleted from packet and ordinal number of packet in terminal node). Ordinal number of packet need for reordering control.

3 PERFORMANCE EVALUATION

One of tasks that can be done with such a model is a choice of effective buffering scheme when the ports' load is asymmetric. The rate of source ports is several times

less than the rate of port connected to handler port. If the fly-by commutation is used, then interconnection line to the handler will stand idle and waiting time for packets from other sources will increase. As a result the line to handler will stand idle during time enough for some symbols transmission after transmission of every one symbol. Using of switching with buffering allows decreasing of high rate lines idle time due to preliminary data accumulation in a buffer. However efficiency of buffering is essentially decreased when the packet size is greater than the buffer size due to the packet tail that is not placed into buffer when its transmission to destination port is started would be transferred with slow rate with it is arrived into switch. The developed switch model allowed to evaluate maximal acceptable packet size when buffer size is fixed or evaluation of necessary buffer size for a given packet size (average packet size and distribution law).

The model could be used for evaluation of a ratio between the switch fabric data channel throughput and the port throughput (interconnection lines throughput). Increasing of switch fabric data channel throughput could be reached by increasing local clock frequency or by increasing of number of bytes transmitted in parallel in a switch fabric data channel. Increasing of the switch fabric data channel throughput in combination with packet buffering leads to increasing packet transmission rate through switch fabric, but the port throughput will be a limitation factor. We obtain next results with using our model. The throughput ratio essentially affects the average packet transmission time when input port load is more than 95%. When the input port load is 99% increasing of throughput ratio from 1:1 to 4:3 allow decreasing the average packet transmission time to 11%. Further increasing the throughput ratio is less effective: an increase of throughput ratio from 4:3 to 2:1 leads to only 5%decrease of the average packet transmission time.