SpaceWire IP
for
Actel Radiation Tolerant FPGAs

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Actel RTAX-S Devices

- Radiation tolerant FPGAs
  - Non-volatile anti-fuse technology
  - Total dose 300 krads
  - SEU 1E-10 Errors/bit/day
  - SEL immune
  - SEU immune to LET > 37 MeV-cm²/mg

- Capabilities
  - Up to 4 million equivalent system gates
  - Up to 500 k ASIC equivalent gates
  - Up to 540 k bits embedded RAM/FIFO
  - Up to 840 user I/Os
  - Four segmentable clocks
  - Flight suitable packages
  - RTAX4000S/SL
Actel RTAX-S Devices

- **RTAX250S/SL**
  - 250 k system gates (30 k ASIC gates)
  - 54 k embedded RAM
  - 248 user I/Os

- **RTAX1000S/SL**
  - 1000 k system gates (125 k ASIC gates)
  - 162 k embedded RAM
  - 516 user I/Os

- **RTAX2000S/SL**
  - 2000 k system gates (250 k ASIC gates)
  - 288 k embedded RAM
  - 684 user I/Os
Actel Block Flow

- Ensure consistent performance
  - When reusing a block of design
  - In a new application

- Place-and-route of original design locked

- Can then be integrated as a design block
  - In top-level of a new project

- New feature within Libero IDE
SpaceWire CODEC Architecture (1)

Transmitter

- TX Data Rate
- Transmit Data
- Time-Code
- Transmit Control/Status

Receiver

- Data/Strobe Out
- Receive Control/Status
- Time-Code
- Receive Data

Data/Strobe In

Link Control

Link Status
SpaceWire CODEC Architecture (2)

- **Transmitter**
  - Serialisation using shift registers
  - Variable data rate
  - Selects next character to send based on
    - Initialisation state
    - Current requests
  - Allowed to send data characters when FCTs are received
    - Each FCT permits 8 more data-characters/EOPs

- **Receiver**
  - Performs receiver clock recovery
  - Decodes input bit-stream
  - Controls receiver buffer credit operations
  - Resynchronises received characters to receive buffer clock
SpaceWire CODEC Architecture (3)

- **Initialisation State Machine**
  - Establishes a connection with other end of link
  - Enables and disables transmitter and receiver
  - Timeout counters for state changes

- **Internal Error Recovery**
  - Error recovery is performed when a link error is detected
  - Recovers the tx and rx data buffers due to link disconnection
    - Transmitter may be in the middle of sending a packet
      - Packet is flushed from transmitter buffer
    - Receiver may have been receiving a data packet
      - Received packet is truncated with an error end of packet
    - Any outstanding FCT characters are added back to space available in receiver buffer counter
SpaceWire in Actel Devices

- Key problem is the clock recovery chain
- In the SpaceWire Receiver
- Hard to guarantee performance
- Clock recovery implemented using XOR
  - Delay of recovered clock must be longer than delay of data

<table>
<thead>
<tr>
<th>DATA-STROBE ENCODING</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data</td>
</tr>
<tr>
<td>D</td>
</tr>
<tr>
<td>S</td>
</tr>
<tr>
<td>CLK</td>
</tr>
</tbody>
</table>
Receive Clock Timing
Skew and Jitter

D ideal

S ideal

D

S

CLK

\( t_{\text{skew}} \)

\( t_{\text{jitter}} \)

\( t_{\text{dclk}} \)

\( t_{\text{hold}} \)

\( t_{\text{ui}} \)
Actel SpaceWire Clock Recovery

- Actel clock tree has large minimum delay
  - Helps avoid race condition
  - Timing tools can then give reliable timing analysis

- Application note
  - “Implementation of the SpaceWire Clock Recovery Logic in Actel RTAX-S Devices”
  - Actel Corporation 2007
SpaceWire Source

SpaceWire RMAP Command

SpaceWire Interface

RMAP Header

RMAP Data

Check Header

Address

Data length

Check Data

Start

DMA Controller

Authorisation Request

Authorisation Grant

Bus Request

Bus Grant

Start Ack

Data

Data

Data

Relinquish Bus

Done

Indicate

User Memory/ RegisterBus

SpaceWire RMAP Reply

RMAP Reply
Conclusions

- Well proven SpaceWire interface
  - Extensively tested by third parties
  - Used in several ASICs
  - Used in many FPGAs
- Guaranteed performance due to “Block Flow”
- RMAP interface to user logic
  - Simplifies design
  - Uses standard packet format & protocols
  - Extensive test & debug equipment available
- Actel radiation tolerant FPGA
- Plenty of room for custom logic to control instruments and other equipment