A SpaceWire Implementation of Chainless Boundary Scan Architecture for Embedded Testing

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Introduction

- Currently Astrium Ltd uses JTAG boundary scan to perform embedded testing.
- This has been successful on missions such as Inmarsat 4 and Skynet 5.
- This presentation proposes a novel boundary scan architecture “Chainless Boundary Scan” (Patent filed) which is well suited to SpaceWire based systems.
- What is JTAG boundary Scan and how does it work?
JTAG Boundary Scan - Background

• JTAG Stands for:
  “Joint Test Action Group”
• The Group was setup in 1985 in Europe (Known as JETAG)
• In 1986, It expanded to include members outside of Europe and hence dropped the ‘E’ from JETAG to become JTAG)
• The IEEE1149.1 std. was approved on the 15th September 1990 and is known as:
  • “IEEE Standard Test Access Port and Boundary Scan Architecture”
• How does boundary scan work?
Boundary Scan Cell

Boundary-scan register formed from ‘silicon nails’ cells.

Memory element called scan-cell

* = OPTIONAL within IEEE Std. 1149.1
Example: Performing interconnect Testing

Boundary-scan register formed from ‘silicon nails’ cells.
Daisy-chaining Boundary Scan Components & Issues

Issues:

- Breaks in the chain
- Connecting many components into small number of chains (conventional test equipment provides 4 Chains).
  - Throughput, management of different logic and different supply levels, redundancy.
Time for a change
Typical SpW based Architecture
“Chainless Boundary Scan”

Test Equipment or Ground Station

Any comms link

BIST Controller

Memory

SpW Router

C1

C2

C3

C4

Target Hardware

SpW

SpW

SpW

SpW

SpW

SpW

SpW

SpW

SpW

SpW

SpW

SpW

Any comms link

Key

Cn = Component n
SpW Router to Boundary Scan Adapter

Host device internal logic (e.g. DSP ASIC) if adapter is not stand-alone.

Block C can either be standalone or form part of either Block A or Block B.
Hybrid Solution

Chainless SpW based Architecture

D1 to D6

Standard Boundary Scan Architecture: D1 to D6

D7
External TAP I/F

C1
C2
C3

Stand-alone SpW Router - Boundary Scan Adapter IP with Boundary Scan Gateable Router (G8R)

SpW

D2
D3
D4
D5
D6

SpW

TAP 1
TAP 2
TAP 3
TAP 4
Spare

SpW

Operator
BIST Controller
Command & Data I/F

Memory

SpW Router - Boundary Scan Adapter IP

Component with standard boundary scan

Components with built-in SpW Router - Boundary Scan Adapter IP

Hybridised Chainless and Standard Boundary Scan Architecture
Conclusion

- Chainless Boundary scan using SpW based architecture provides the following advantages:
  - Tests can still be performed even after one or more components have been configured in functional mode or if a failure of a component occurs.
  - The boundary scan vectors can be transported across the network in macro-command and data packets without having to translate them into IEEE1149.1 signal compatible format.
  - Allows in-orbit testing possible as no additional test infrastructure is required.