Integrated Development Tools Suite for the SpaceWire RTC ASIC

SpaceWire Test and Verification
Dundee, 19 September 2007

Walter Errico
Aurelia Microelettronica Srl
Via Vetricina, 11 - 55049 Viareggio (Italy)
phone: +39 0584 388398
e-mail: walter.errico@aurelia-micro.it
URL - http://www.aurelia-micro.it
The SpW RTC Development Suite is a set of mainly HW and SW tools dedicated to the SpaceWire Remote Terminal Controller device.

Objective:
- To lead the RTC users to the full exploitation of RTC device with a "quick start" approach.

Features:
- Complete → All the RTC functionalities are addressed.
- Self Contained → No additional laboratory instrument is needed
- Flexible → Open to possibility of HW, SW & FM upgrade and customization

(*) ESA/Aurelia Microelettronica contract no. 20335/06/F/VS
**HW tools**

- Two-boards:
  - **PCI-SpW/CAN**
  - **RTC Test-Bed**

- Communication Cables (SpW, CAN, serial, parallel)

- Power adapter
PCI-SPW/CAN and RTC Test-Bed boards

SpW RTC Development Suite

- PCI-SpW/CAN
- FLASH 64Mbit
- 8bit uC.
- JTAG
- Flat Par. Con.
- FPGA

RTC Test-Bed

- JTAG
- ADC
- DAC
- SRAM
- SRAM
- SRAM
- FLASH
- EPROM
- Power Supply
- SpW RTC ASIC
- FIF
- FIF
- clock
- clock
- D.9
- D.25
- Power Supply

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PCI-SpW/CAN board

- FPGA Based PCI Peripheral Board
- Large Altera Stratix FPGA 5/6 Million Gates, 90nm technology
- PCI Master/Slave interface with DMA capability
- Two SpW links up to 400 Mbit
- Two 16-Mail-box CAN controllers
- Custom on board FPGA reprogramming solution
PCI-SpW/CAN FPGA Block Diagram

- Based on AMBA AHB
- PCI AHB Bridge
- A-CAN16b Controllers
- A-RMAP-SpW modules
- Service Block (Memory on Chip + GPIOs + Reset/DSU)
A_RMAP-SpW
RTC Test Bed

- Desktop case
- Autonomous power supply chain MCGA 349 Socket for SpaceWire RTC ASIC
- Two clock oscillators
- DC/DC converter
- SRAM, FLASH, EPROM on board
- Two FIFO components
- DAC + ADC devices
- Two CAN transceiver+connectors
- Two micro D9 connectors for SpaceWire
- Serial and Parallel standard Connectors
- Hot plug mezzanine option for FIFO and ADC/DAC interface
RTC Memory Bus

- 16 M byte SRAM
- 8 M byte Flash or
  128 K byte EPROM
  on ROM space 0
- 8 M byte Flash on
  ROM space 1
FIFO interface

- Two 16k x 9 FIFO mounted in loop
- Possibility to disconnect FIFO devices in favour of custom mezzanine solution
RTC ADC/DAC interface

- DAC and ADC on board
- Loop-back option with external cable
- Possibility to disconnect devices in favour of custom mezzanine solution
**SW tools**

**SUITE SW Library**

- Unique agile Application Programmer Interface for all the links (SpW, CAN, GPIO)
- SpW RMAP support for RTC remote control

Collection of **Sample procedures** to utilize all the RTC interfaces

- Based on RMAP remote control
- Running from a LINUX test PC
- Written in C‘and PERL‘languages
Suite SW library

ApplicationLayer

RemoteProcedureLayer

TransferLayer

PCIDriverLayer

HWLayer(PCI-SPW/CAN)
REMOTE Control Sample: Boot from on chip memory
REMOTE Control Sample: Boot from on chip memory

- PCI-AHB Bridge
- Service & On-Chip Memory
- FPGA
- RMAP-SPW
- SPW Link
- Parallel Cable
- SPI Bus
- AHB Bus
- On-Chip Memory
- LEON2-FT
- DSU
- On-Chip Memory

Reset & DSU controls
LEON2-FT registers control via DSU
On chip memory boot code upload

International SpaceWire Conference 2007
REMOTE Control Sample: ADC measurement
REMOTE Control Sample: ADC measurement
Conclusions

The RTC ASIC is expected for early 2008.

The SpW RTC Development Suite will be available soon to allow the users to evaluate the new device features and to start developing applications on it.