

A Methodology and the Tool for Testing SpaceWire Routing Switches

Session: SpaceWire test and verification

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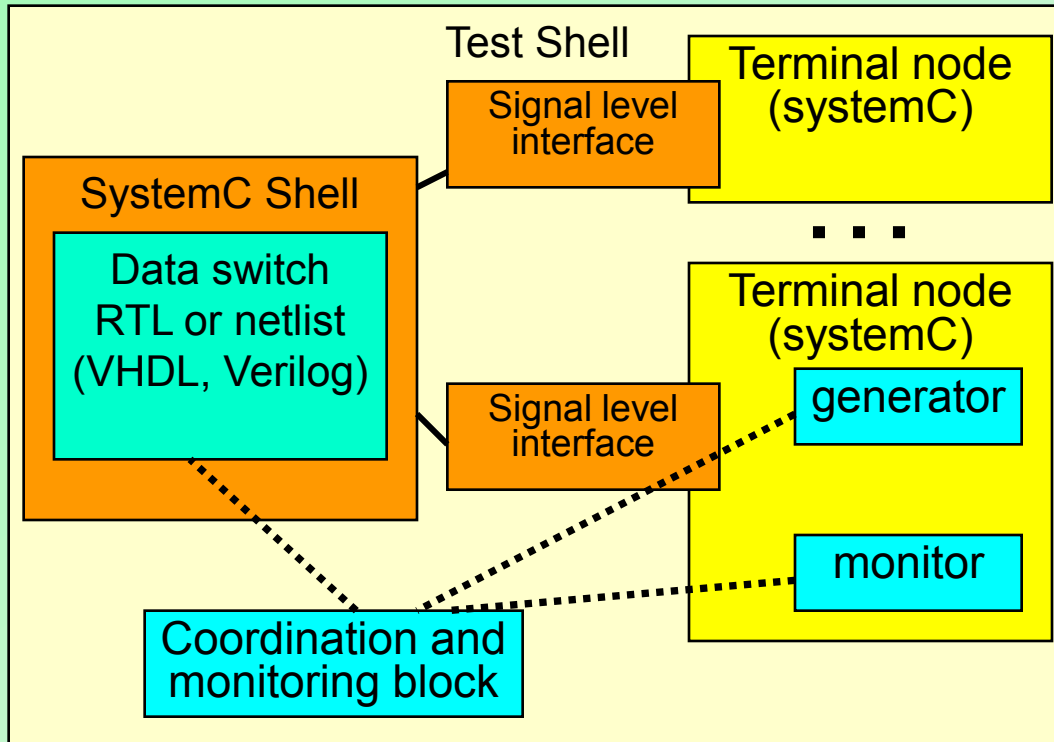
Requirements to tool for testing SpaceWire Routing Switches

- Could be used for verification of different switches (with different ports number, with different configuration scheme, different program-assessable components)
- Could be used for system level, RTL level, post-synthesis level switch models
- Could be used for verification single switches, single switches in network and whole network
- Allow validation of multicasting and adaptive routing functions
- Easy for using

Verification methodology

- Division stage of giving input test vectors and fixing result outputs values from result verification stage. This division need because correct sequence of packets to one terminal node from different terminal nodes may be different (it is not possible to predict it), and because through adaptive group routing packet that send to one terminal node from group could be received by other terminal node from this group.
- Including special information in packet payload (for generation unique packet identifier). This mechanism allow easy examination packet transmission correctness not only for one switch but for whole network. Packet identifier structure look like RMAP packet format but is more compact that allow shorter packet payload length. (It is important because some switching failures are found only for short packets and not in all cases RMAP is used)

Suggested Test shell as verification tool



Test shell includes:

- Data switch models (SystemC, VHDL, Verilog)
- Terminal nodes models (SystemC)
- Interconnection lines
- Coordination and monitoring block (SystemC)

Shell main file (SystemC) – perform component's generation and interconnection topology construction accordingly configuration files

configuration files:

Includes user defined parameters

**This Test Shell orient to Cadence simulation tools
(ncSim, Simvision: IUS5.1 – 5.7 design flow)**

Test shell main features

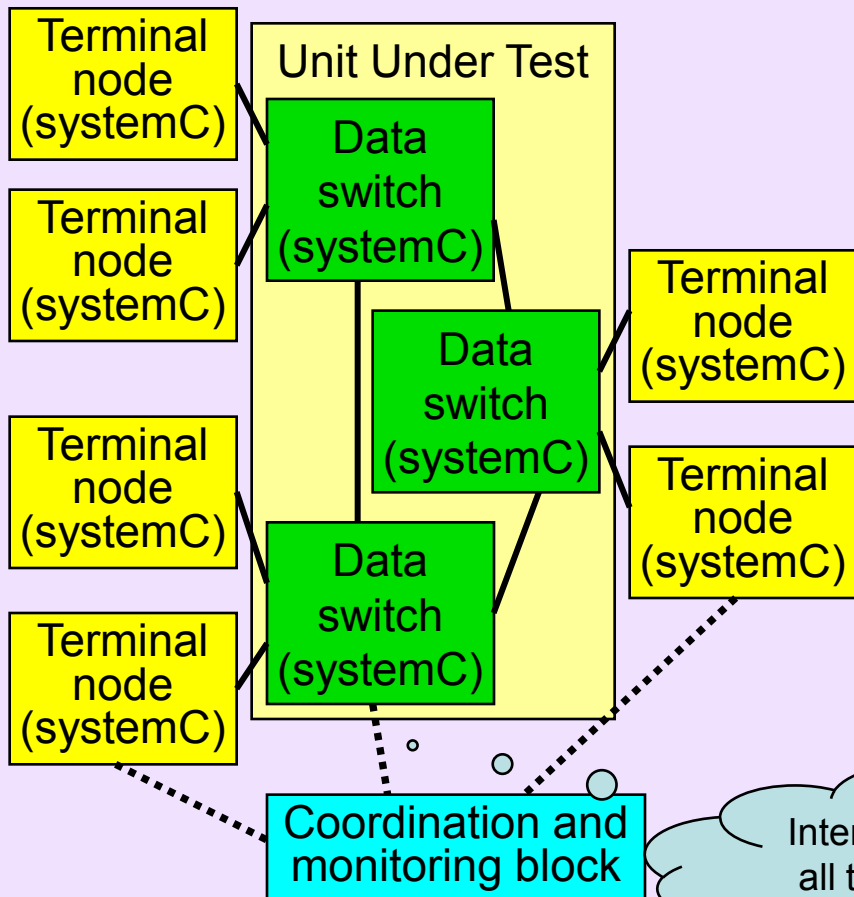
- Allow validation of multicasting and adaptive routing functions
- Could be used for single switches (number of ports is user defined) or for switch based networks (number of switches and topology are user defined)
- Could include System Level (SystemC), RTL or post-Synthesys Level (VHDL, Verilog) switch models
- Automatically configurable based on user defined parameters

Test shell examples (System Level)

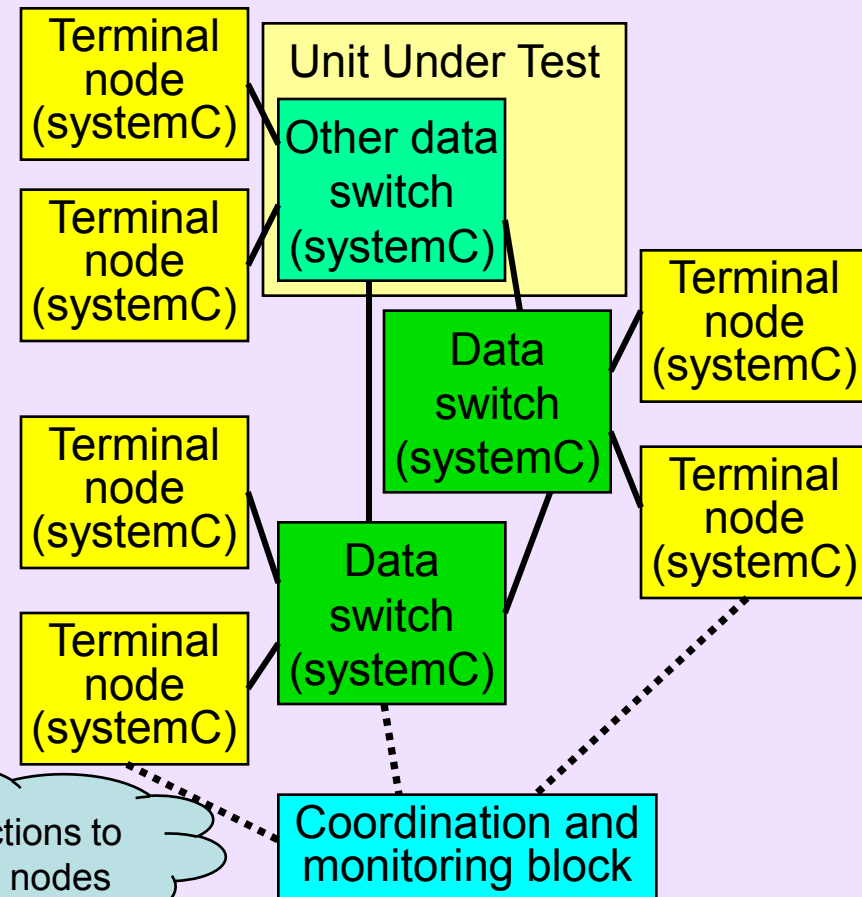
For whole network verification

For one switch in network verification

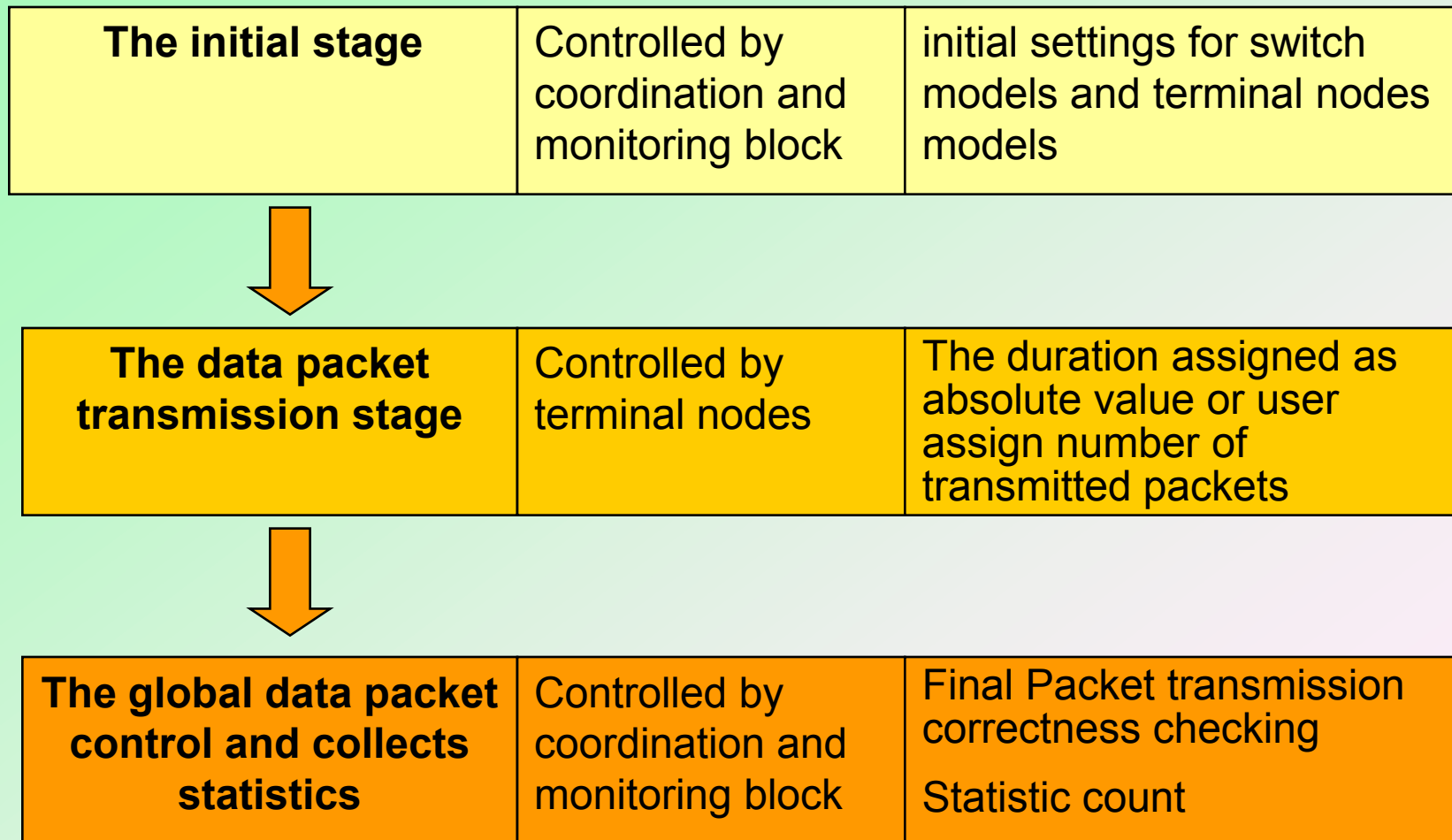
Test shell(systemC)



Test shell(systemC)



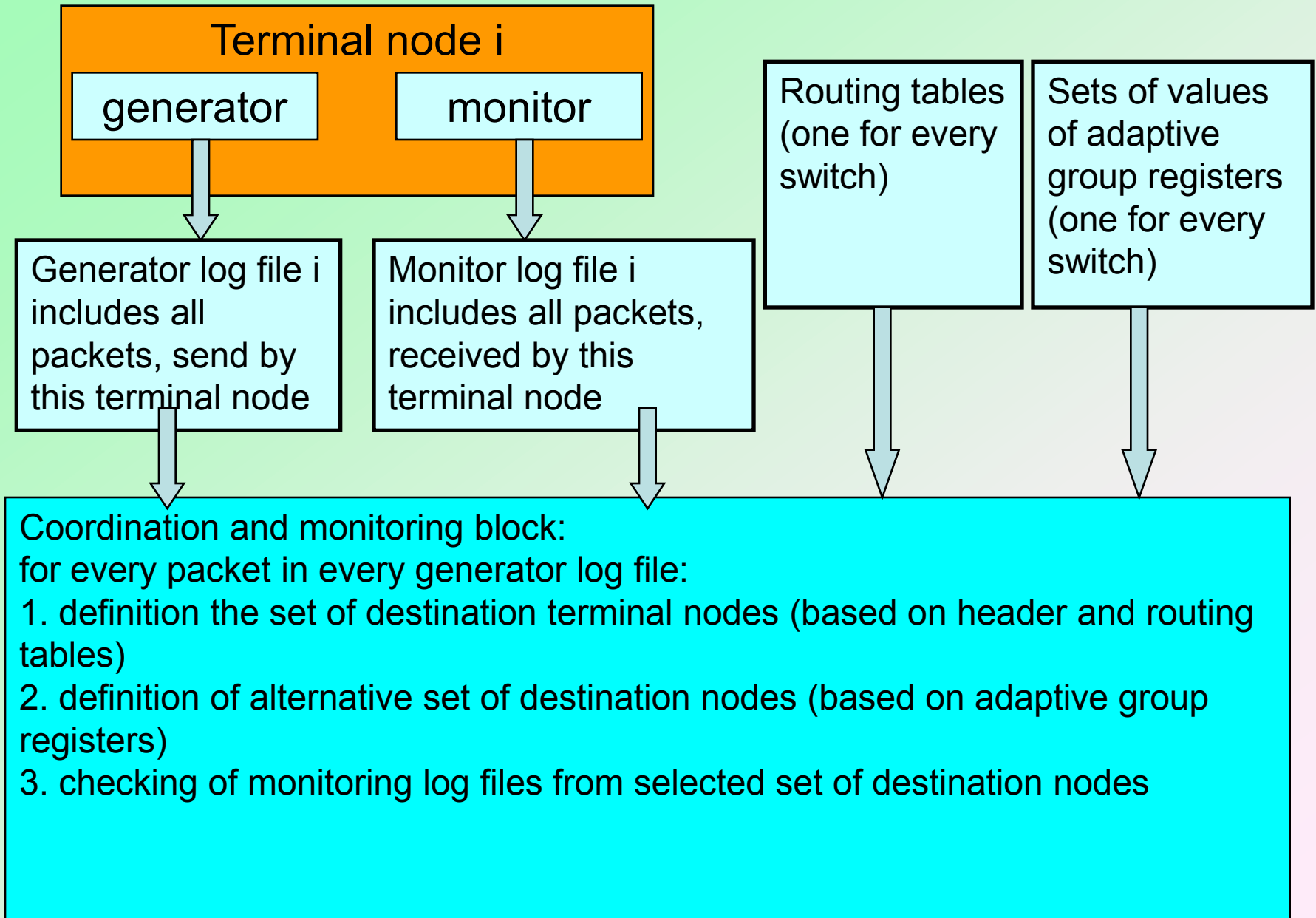
Test shell work process stages



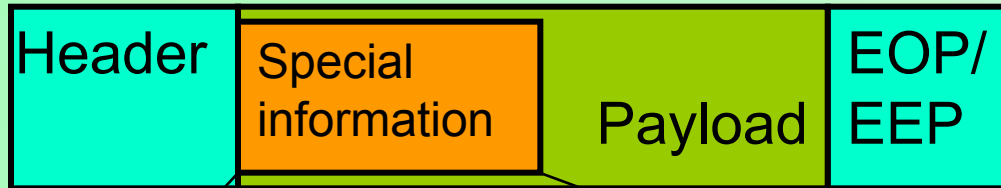
Examples of verification aspects

- packet header must be excluded from the packet or not excluded according routing table settings
- packet contents and end-of-packet symbol must follow without changes
- The set of ports, which received this packet, must correspond to its address and adaptive routing settings

Data packet control description

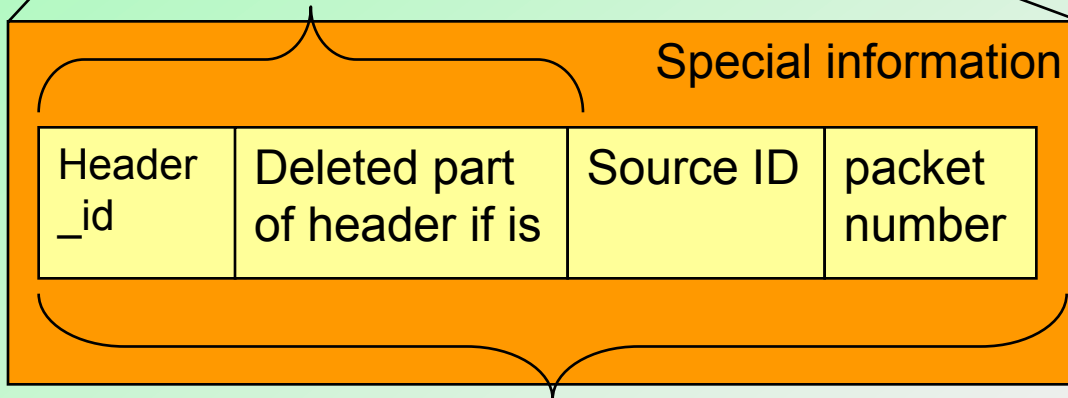


Test packet format



Using of special information allow minimization of comparison operations during data packet control stage

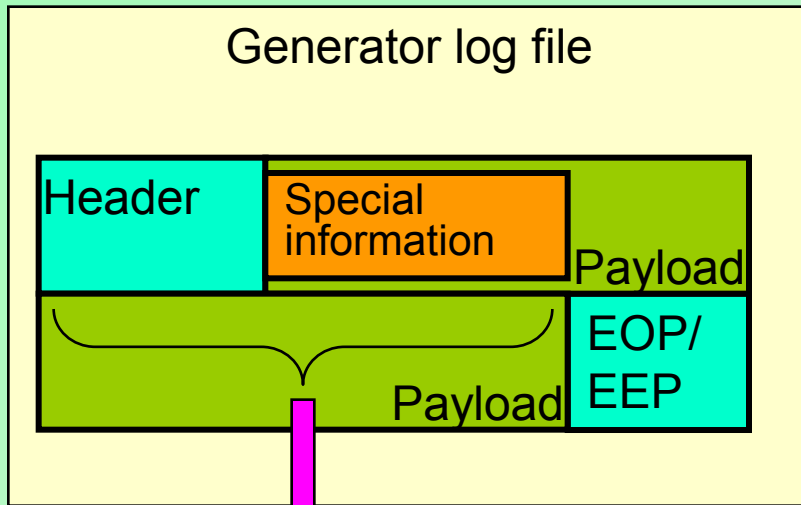
Used for header reconstruction



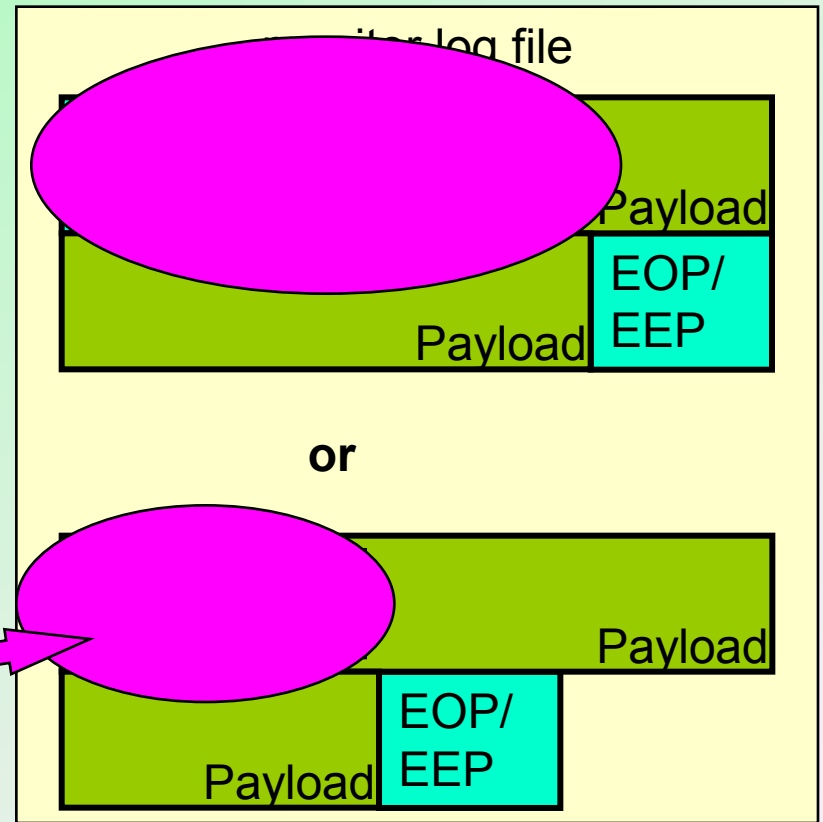
This information is added into packet by terminal node generator and

used by coordination and monitoring block during The global data packet control stage

Checking of monitoring log files from selected set of destination nodes



Coordination and monitoring block:
1. packet identifier generation
2. looking for the packet identifier in monitor log files



The packet identifier includes a part of header that should be received (if is) and special information). It is unique. (Identifiers for all generated by all terminal nodes packets are different)

Performance Evaluation

- Choice of effective arbitration method
- Choice of effective buffering scheme
- Choice of a ratio between the switch fabric data channel throughput and the port throughput
- And other tasks

Thank you!