"MCFlight™"– the Chipset for Distributed Signal Processing and control with SpaceWire Interconnections

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Dundee, Scotland, UK

AGENDA

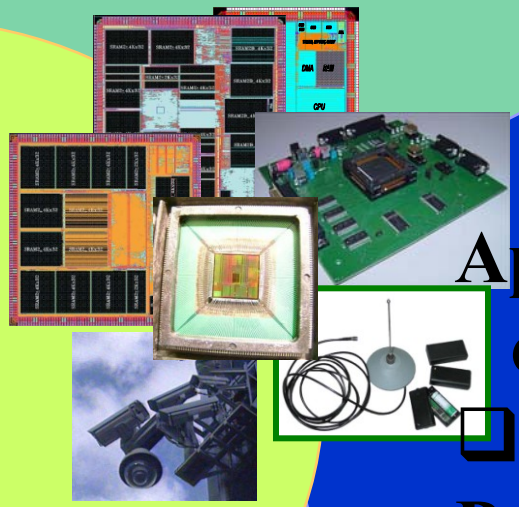
- ELVEES's market segments
- Innovative "MULTICORE" Platform for the "Digital/Analog" SOC/ASIC design
- Parameters and architecture of the MCFlight Chipset for the SpaceWire based distributed aerospace systems
- The MCFlight examples for the application on-board system
- Conclusions

Some ELVEES Company speed facts

- Fabless R&D microelectronics center – the leading Russian MultiCore SoC and DSP chips developer;
- Was created in 1990 as a part of major in USSR space electronics "ELAS" Corp.
- In 1974 - the first in the USSR CMOS microprocessor, only 2 years after INTEL Corp.;
- More than 400 developed chips; 6-9 months chips Design Flow,
- ~207 employees with VLSI & embedded systems experiences: average age – ~ 37 years
- HQ - Moscow, Zelenograd district ("Russian Silicon Valley"), ELVEES's departments in USA and Israel

ELVEES market segments

ELVEES proprietary SOC Platform “MULTICORE”



Embedded, security systems

Application specific chipsets for:

- **IP-Camera & Image Processing;**
- **Fusion Sensors;**
- **Telecommunications;**
- **Commercial space**

World class ELVEES's proprietary "MULTICORE" platform for programmable SOC/ASIC design

Applications

SOFT

Algorithms

Software Tools

Application Software

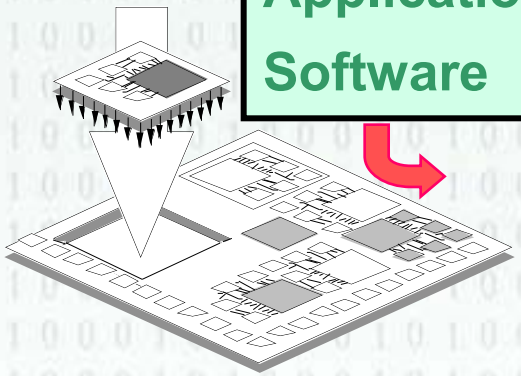
SOC DESIGN TECHNOLOGY

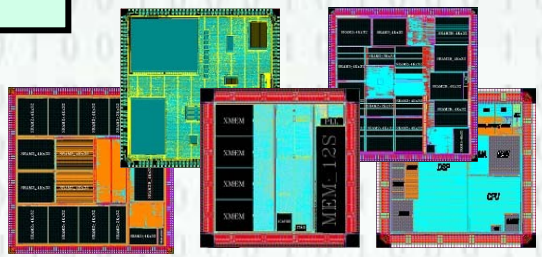
HARD

Architecture

IP-CORES LIBRARY

6-9 MONTHLY design flow

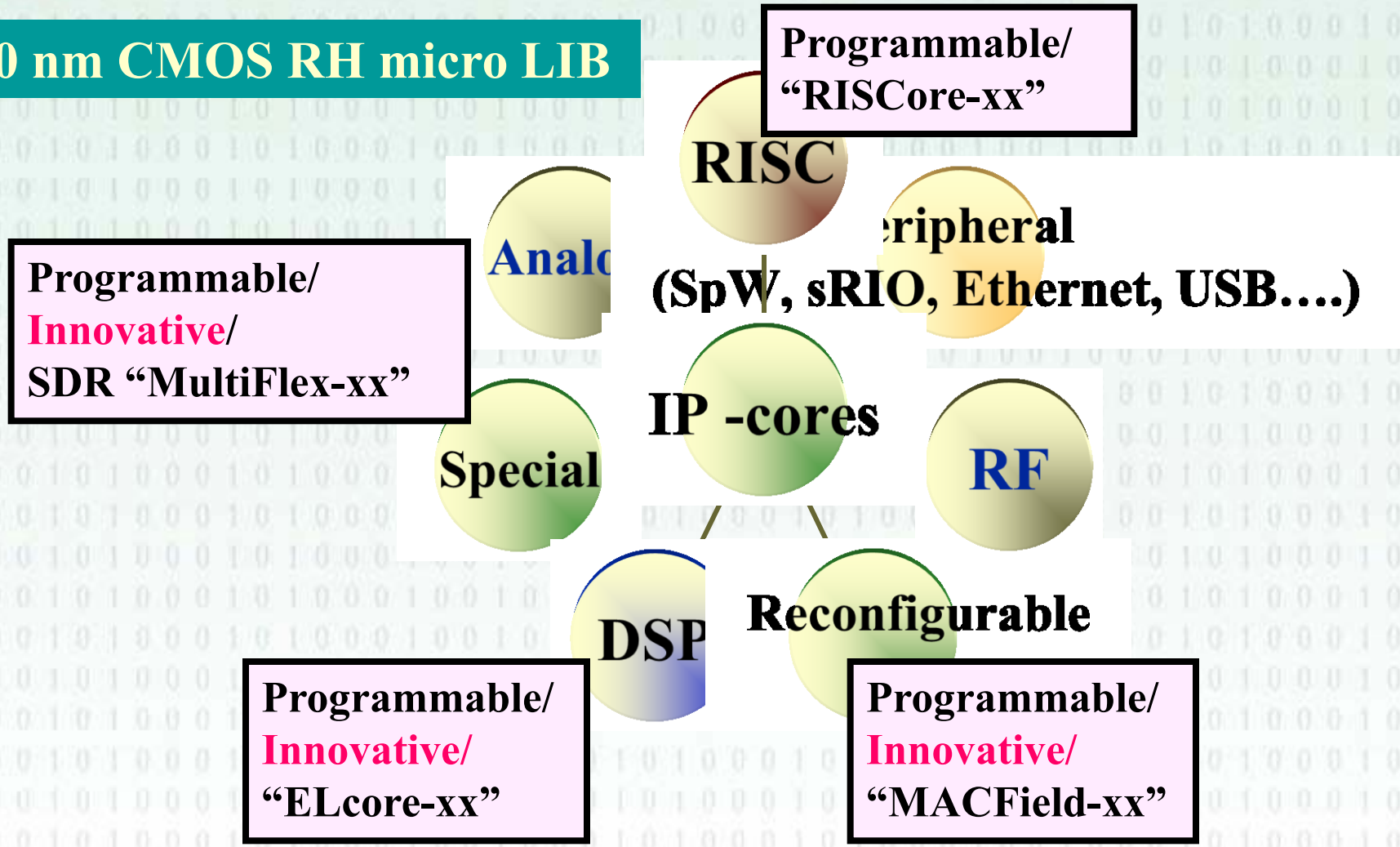




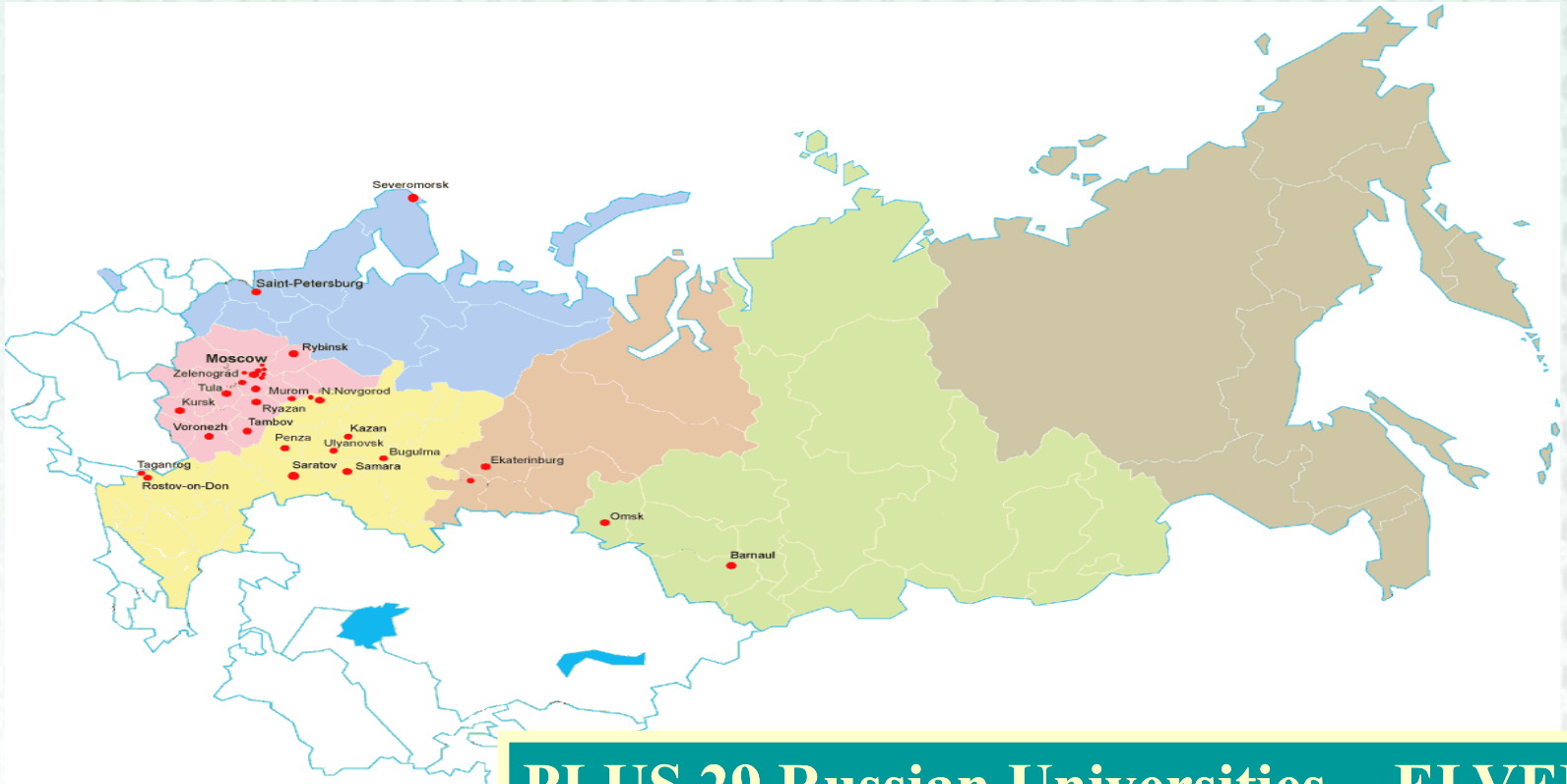
Chips examples

“MULTICORE” hard & soft “silver/gold” IP-Cores Library groups for 250-130nm

250 nm CMOS RH micro LIB



ELVEES's Customers > 80 Russian firms in semiconductor and technology area apply the testing/verification and create thousands program lines for the MULTICORE platform



PLUS 29 Russian Universities - ELVEES's partners Training programs on the "MULTICORE" Tools base

ELVEES's "MULTICORE" platform the general conception

❑ Programmability:

- ✓ very short program code (in the 8-10 time (vs. ADI and TI DSP Chips);
- ✓ powerful module SW/HW Tools (MCStudio™);
- ✓ 4 groups programmable IP-Cores;

❑ Scalability and flexibility at the levels of:

- ✓ IP-cores - SIMD/MIMD/ pipeline/ superscalar IP-cores extensions;
- ✓ chips - multiple processors on the single silicon (nRISC + kDSP + l SDR-cores+ m Reconfiguration-cores);
- ✓ systems: multidimensional systems configurations on the base SpaceWire and Serial Rapid IO standards (as RIO Trade Ass. Member);

❑ Commercial CMOS technologies (for analog, RF - microcircuits and radiation tolerant chips);

❑ Proprietary "Gold" and "Silver" IP-cores Library SOC integration in Chips and World level of IC characteristics (Hundreds GOPs, Tens GFLOPs)

Achievements on the SpaceWire technology development in Russia

- Creation of the complete IC chipset MCFlight ™ and SpaceWire Controllers IP - cores libraries (ELVEES RnD, MiT) on basis SpaceWire and Russian platform MULTICORE;
- The Signals Images processing units and application software development for space applications on the MCFlight ™ basis (RnD firm “Submicron”, Institute Of Space Research, Russian Academy of Science and others Russian equipment developers).
- The MCFlight based software development on the base OS Linux (ELVEES RnD, MiT)

“MCFlight™” - the 1-st MULTICORE platform based radiation tolerant chipset with Space Wire Links (ELVEES RnD, MiT)

MC-24R,
Dual Cores (RISC+DSP) DSP-mP, 600 MFLOP/s

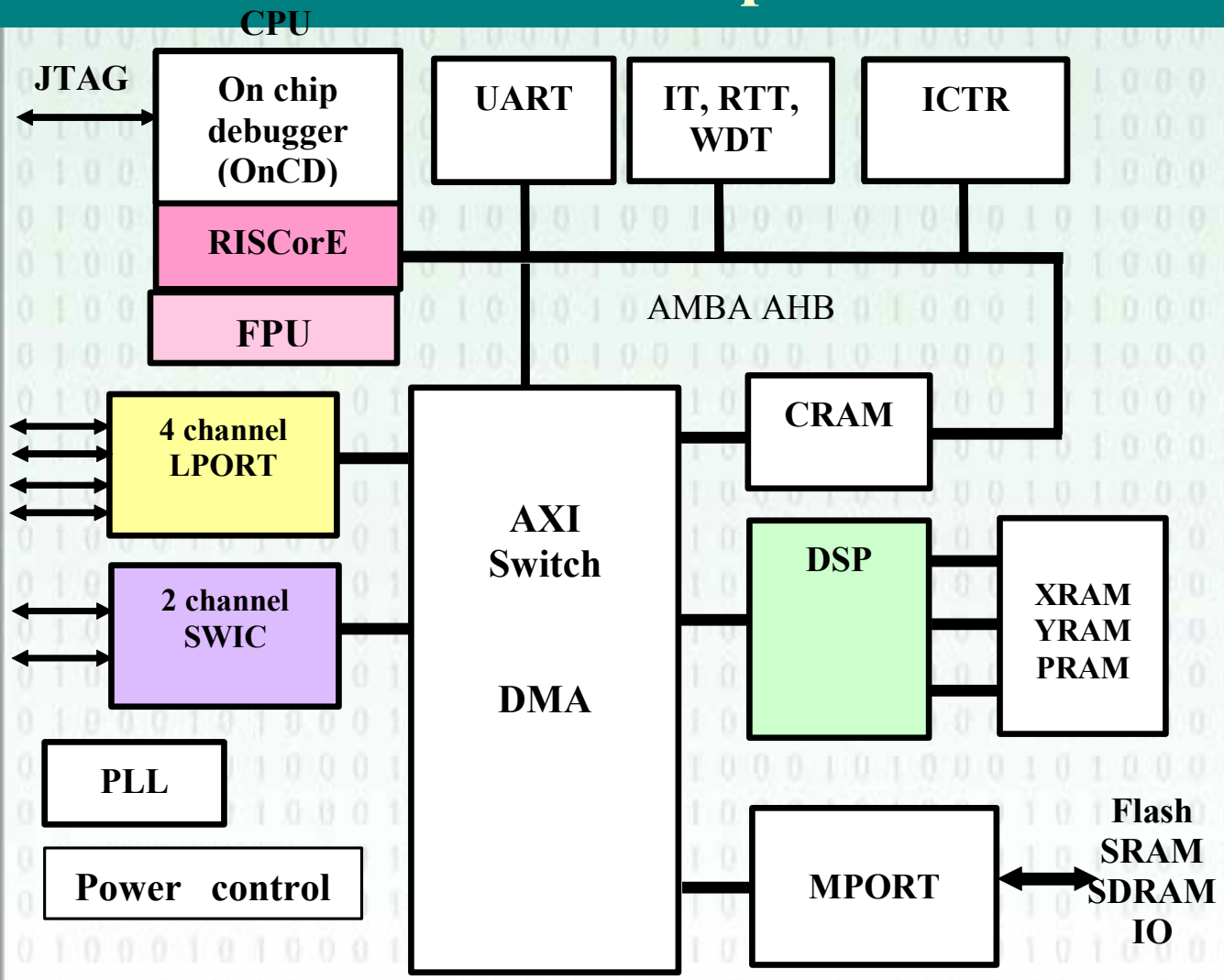
MCB-01,
4 -channel Space Wire/ PCI adapter

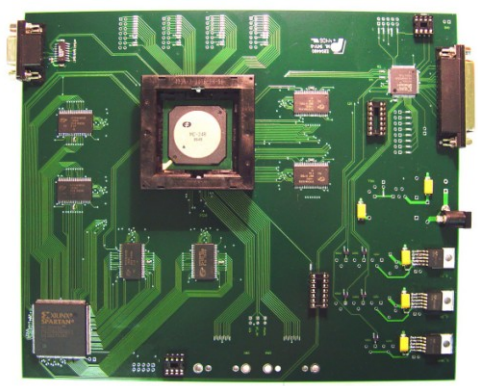
MCK-01,
16-channel Space Wire Router with build-in 32b CPU

MCT-01,
Remote controller 120 MHz, 64-bit FPU

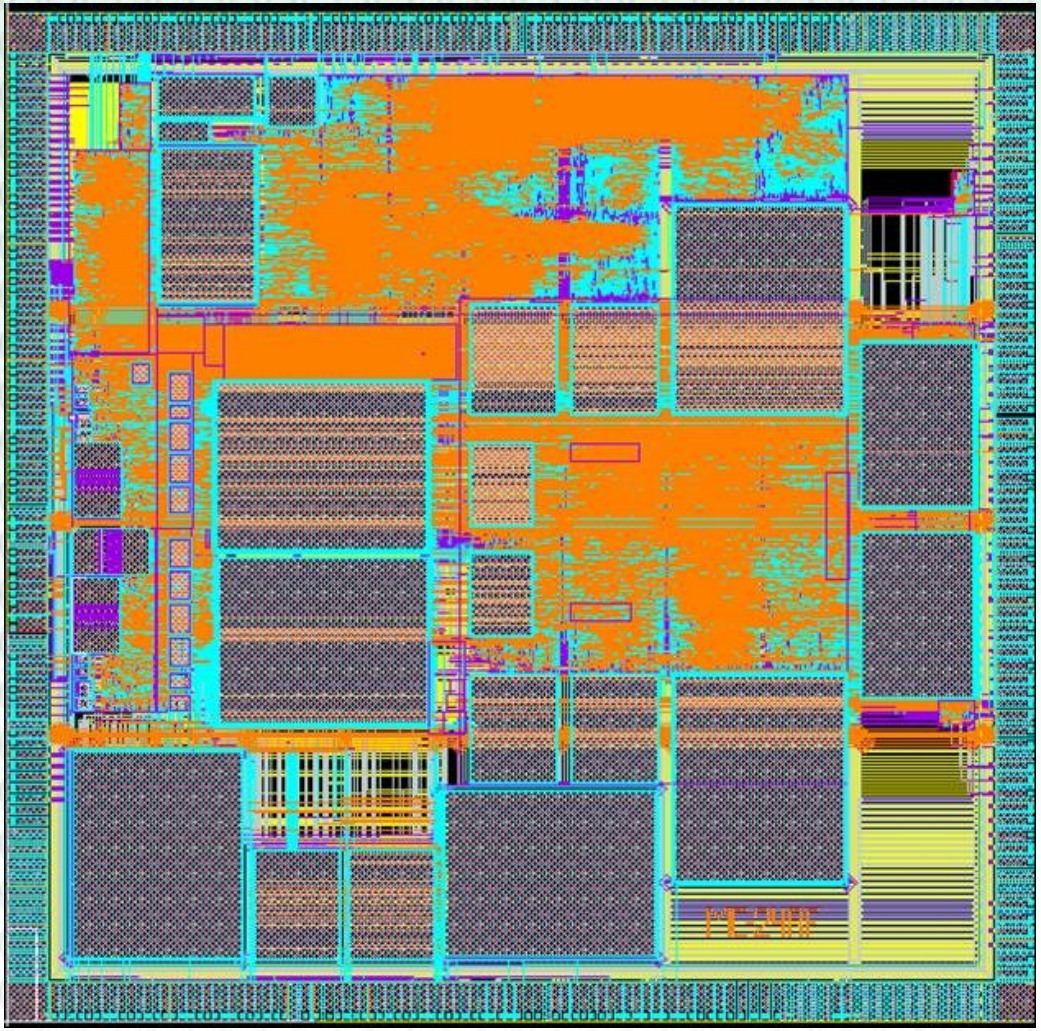
RAM –R,
SRAM 4 Mb (512W*8b), 15ns

MC-24R – 600GFLOPs dual cores RadHard DSP-microprocessor with SpaceWire Links





MC-24R Rad Hard by Design layout

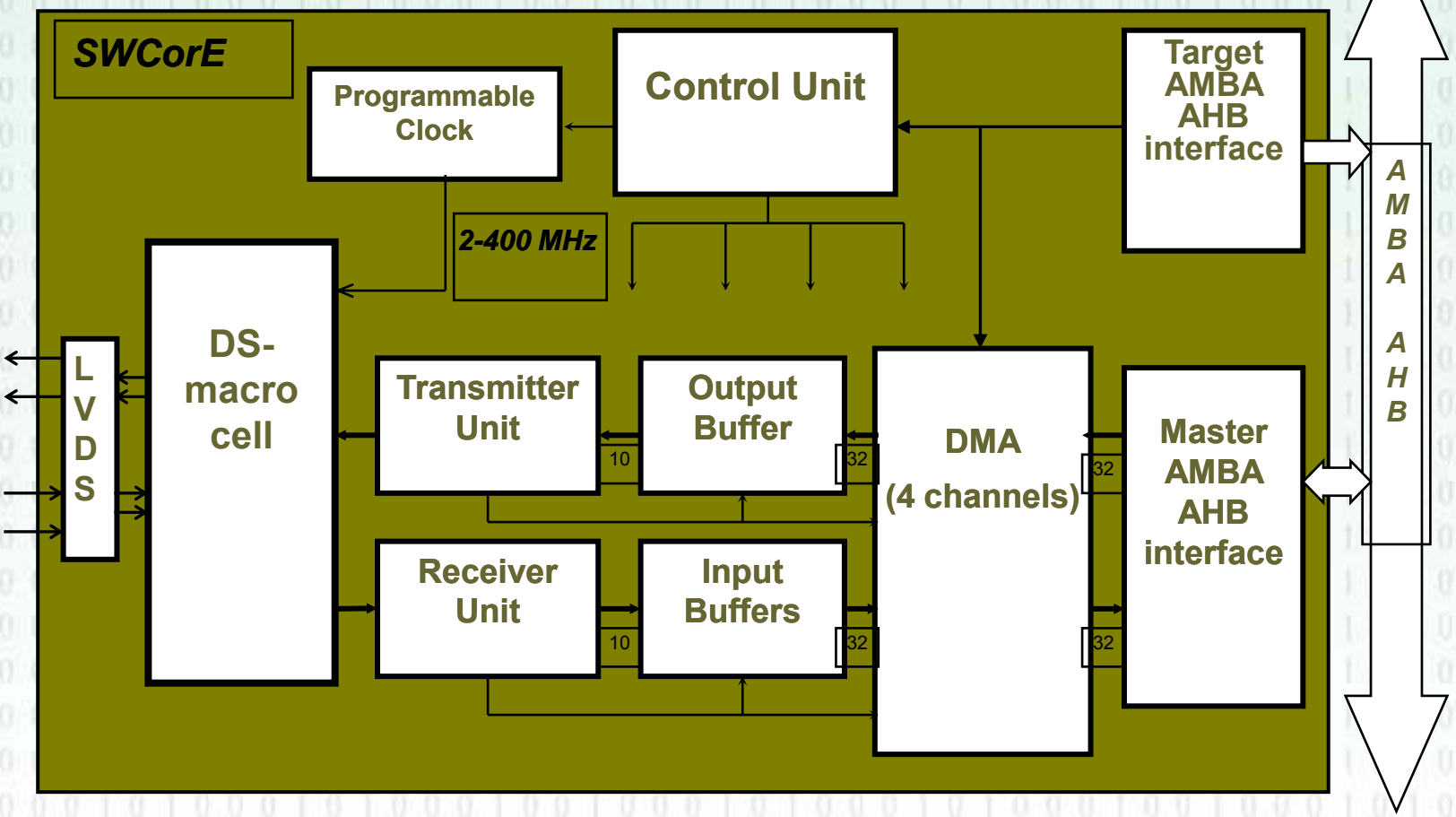


- 250nm, 6 metalas
- "Rad Hard by Design" on the base of the special micro libraries, special architectural and topological decisions
- 12 x12mm*mm

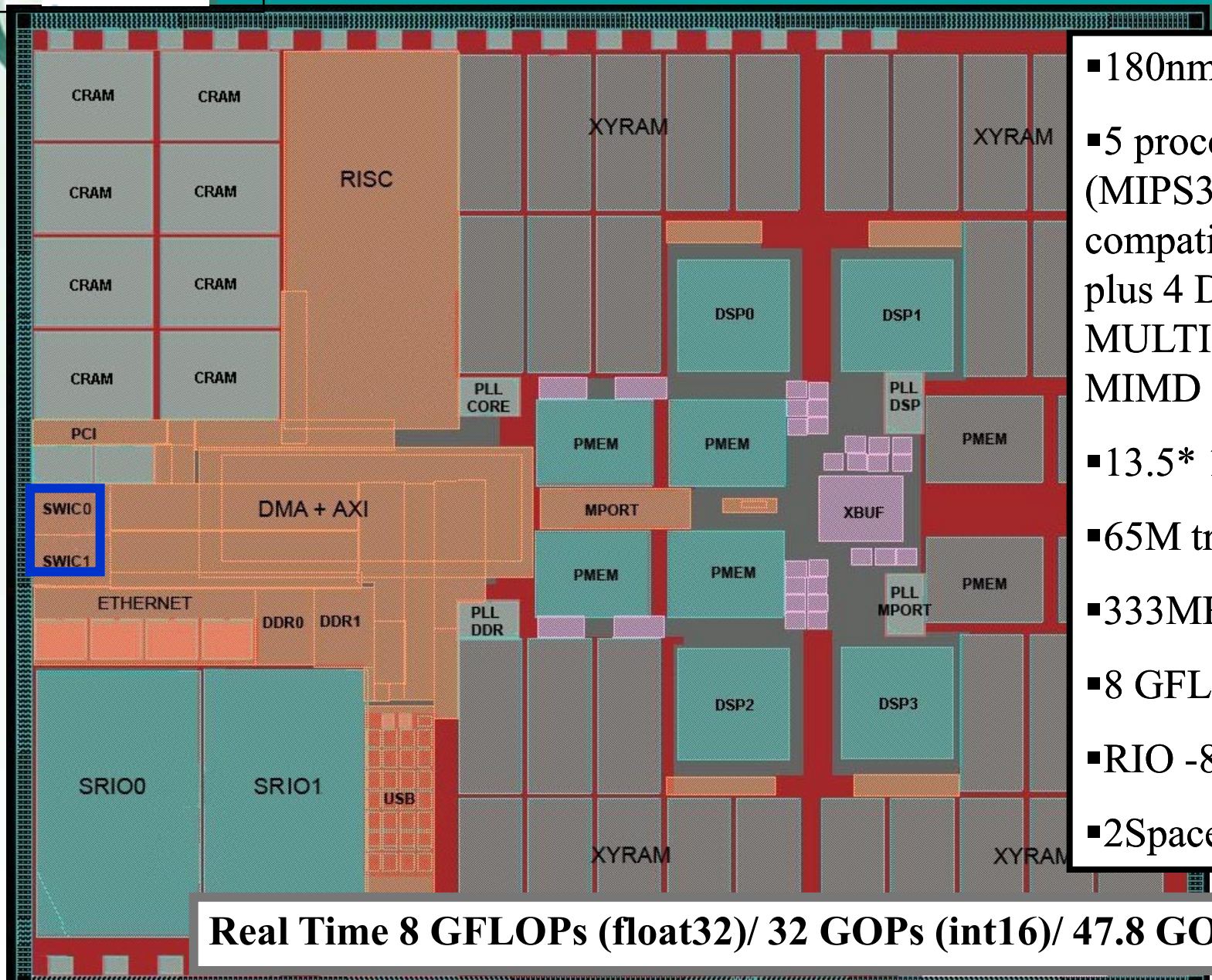
MC-24R parameters

- 250 nm, 6 metals; 2.5V@ core, 3.3V@ peripherals, HSBGA416
- 2 channel SpaceWire, ECSS-E-50-12° standard;
- data rate – 2 – 400 Mbps thought the cables and connectors specified by standard; embedded LVDS ANSI/TIA/EIA-644(LVDS) transceivers;
- two dual processor cores MIMD architecture :
  - RISC core (MIPS32 computable based on “MULTICORE” IP library, TLB) with 32/64 bit FPU in IEEE754, HW MUL/DIV/SQR;;
  - 2SIMD DSP “ELcore28” core;
  - 12Channels “ intellectual” DMA –controller;
  - 2.5 Mb internal memory; all blocks of the memory are protected by modified Hamming code with correction of single and detection double errors;
- peak performance - 600 MFLOPs (100MHz, - 60 - +85 C); several instructions /clock; parallel processing and Load/store;
- Peripherals: UART, MEM Port with SRAM/ SDRAM/ FLASH/ ROM controller, JTAG IEEE 1149.1, 2 SHARC-compatible links/GPIO, Interrupts
- power consumption control: (MHz/mW): 0/25; 10/125; 80/750; 100/1100
- radiation tolerant for aerospace applications
- On Chip Debugger; Software: Linux2.6; RTOS QNX 6.3, MCStudio Tools

“Soft” (Verilog, VHDL), “Hard” and “Firm” (FPGA-based) SpaceWire controller IP -cores (SWIC_xx™) set



SpaceWire and sRIO based MCF-01 layout



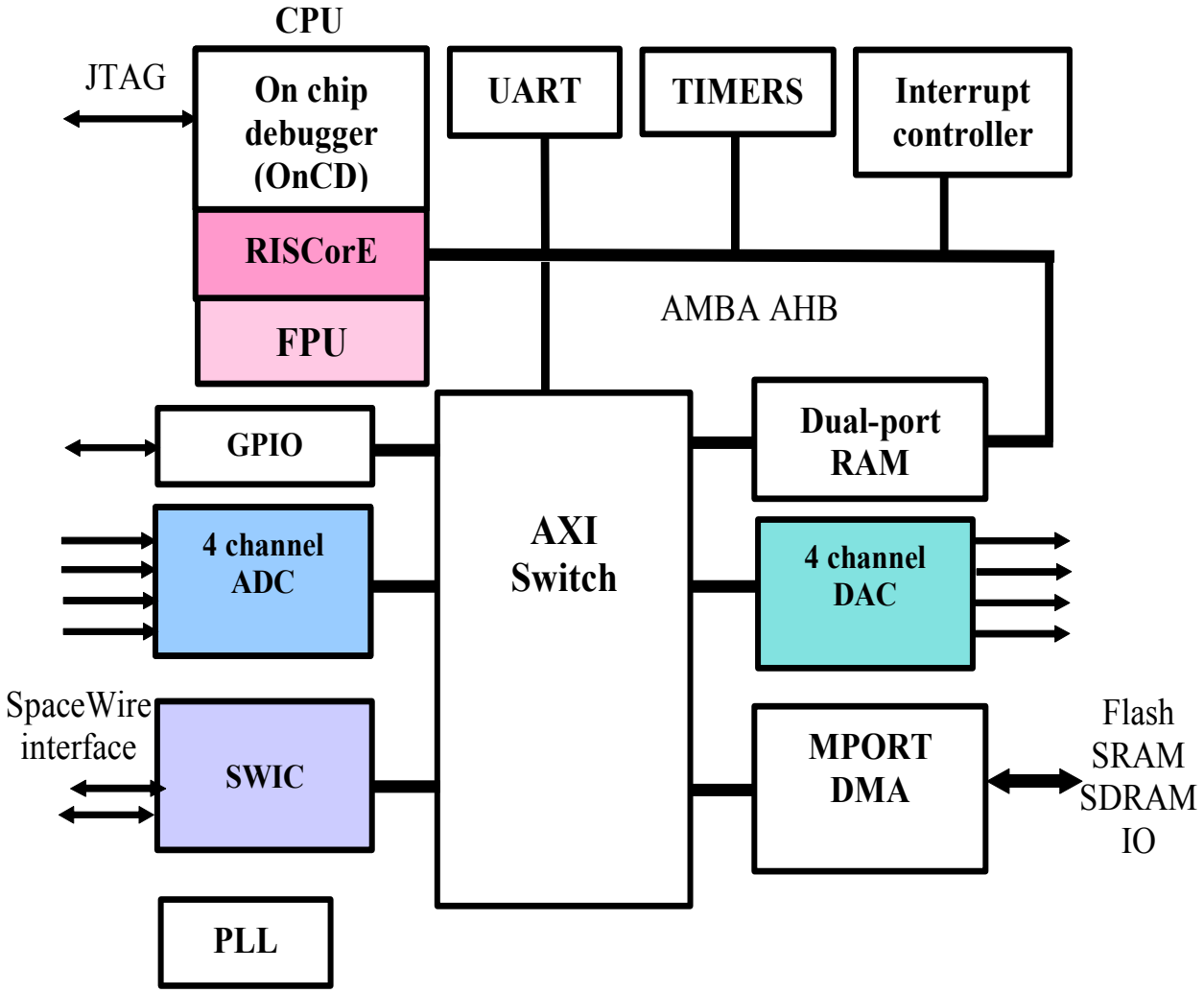
- 180nm, 6 metals
- 5 processors : (MIPS32 ISA compatible RISCore plus 4 DSP cores) MULTICORES MIMD architecture
- 13.5* 16.5mm*mm
- 65M transistors
- 333MHz
- 8 GFLOPs
- RIO -8 Gbps x 2
- 2SpaceWire links

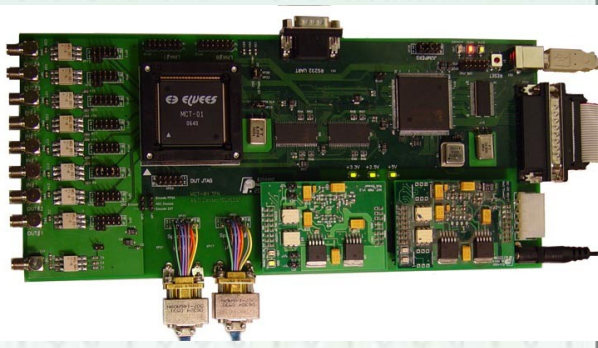
Real Time 8 GFLOPs (float32)/ 32 GOPs (int16)/ 47.8 GOPs (int8)

ELVEES's DSP Multicore Chips with SpaceWire links Vs. Analog Devices Tiger SHARC DSP chips

DSP chip, firm	ADSP-TS101, ADI	ADSP-TS201, ADI	MC24R, ELVEES	MC0226, ELVEES	MCF-01 ELVEES
Clock Speed, MHz	300	600	100	120	333
Design rules, nm	130	130	250	250	180
Top performance (int 16), OP/s	7300	9600	1600	3840	32000
Top performance, GFLOP/s	1800	3600	600	1440	8000
FFT-1024, complex, FLOAT 32 (mcs/clocks)	32.78/ 9835	15.64/ 9384	103/ 10300	42.9/ 4292	6.3/ 2100
FFT-1024, complex, int 16 (mcs/clocks)	18.33/ 5555	7.75/ 4697	52.3/ 5228	18,2/ 2179	3.1/ 1050
FFT program code length (in 32b codes) *) IEEE754	thousands	thousands	hundreds	hundreds	hundreds
SAR task , float 32 (mcs /clocks)	126.6/ 37992	66.9/ 40167	231.3/ 23134	96.4/ 9641	14.4/ 4820
SAR task , int 16 (mcs /clocks)	N/a	N/a	125.0/ 12500	44.5/ 5210	7.8/ 2605

MCT-01 (SpaceWire Remote controller)



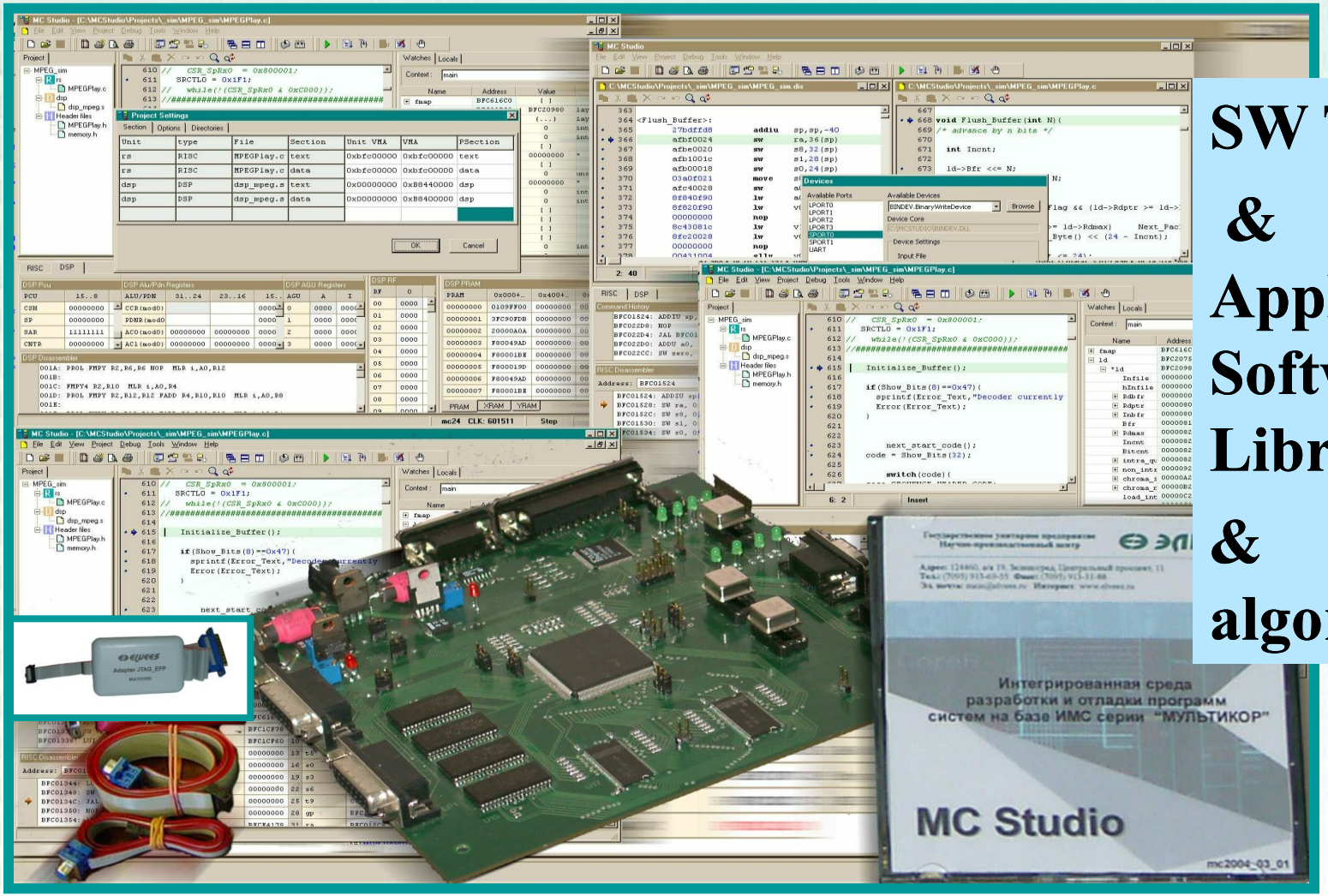


SpaceWire

MCT-01 parameters

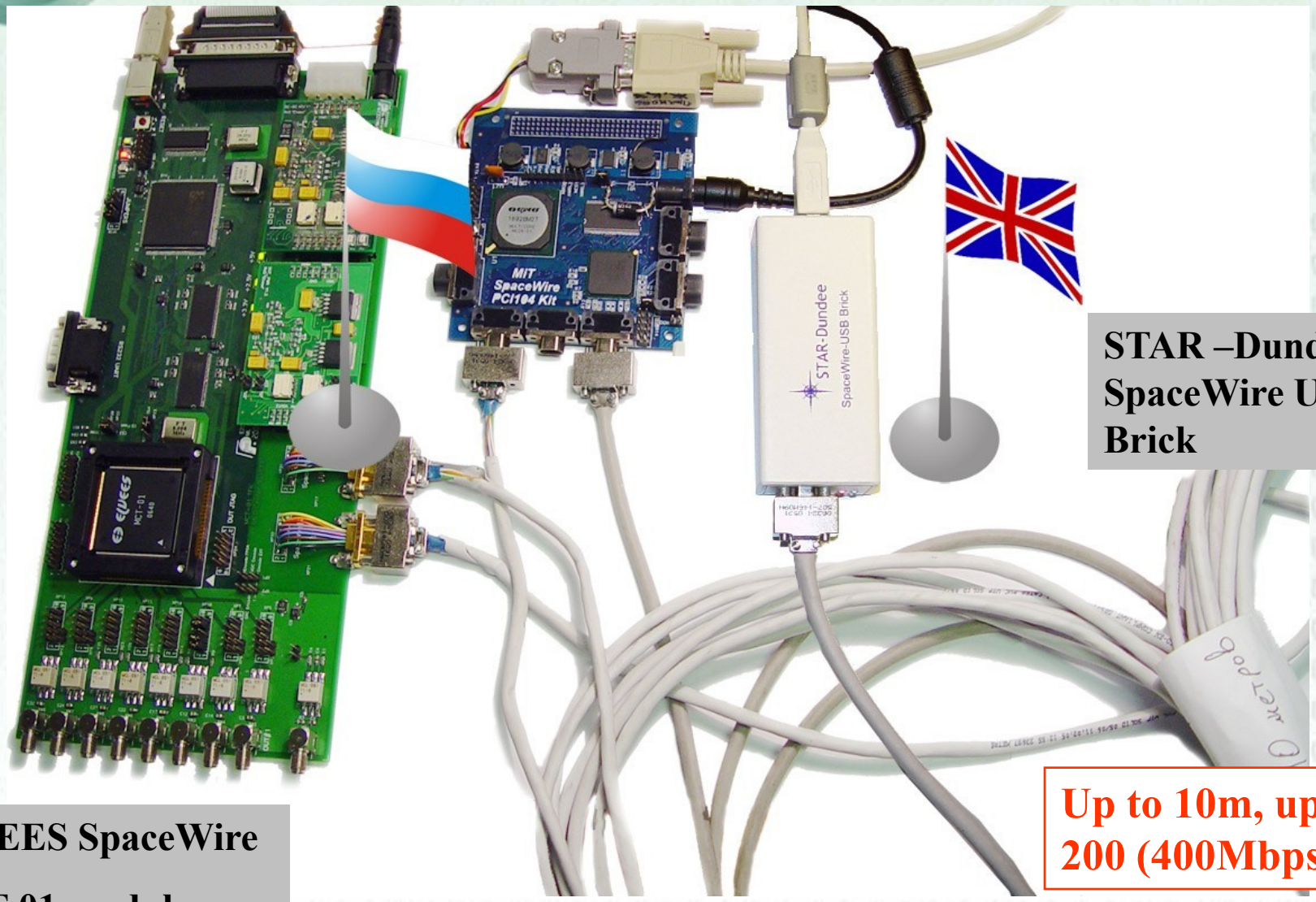
- 250 nm, 6 metals; 2.5V@ core, 3.3V@ peripherals, PQFP-240
- 2 channel SpaceWire, ECSS-E-50-12° standard;
- data rate – 2 – 400 Mbps thought the cables and connectors specified by standard; embedded LVDS ANSI/TIA/EIA-644(LVDS) transceivers;
  - RISC core (MIPS32 computable based on “MULTICORE” IP library, TLB) with 32/64 bit FPU in IEEE754, HW MUL/DIV/SQR;;
  - 16 Channels DMA –controllers;
  - 1.3 Mb internal memory;
- peak performance - 120 MOPs (120MHz);
- Peripherals: UART, MEM Port with SRAM/ SDRAM/ FLASH/ ROM controller, JTAG IEEE 1149.1, 2 SHARC-compatible links/GPIO, Interrupts, ADC/DAC
- test examples are manufactured, tested and verified comparing with and an international implementation of SpaceWire;
- power consumption control: (MHz/mW): 0/12,5; 10/90; 80/550; 100/675
- On Chip Debugger; Software: Linux2.6; RTOS QNX 6.3, MCStudio Tools

Tools: SDK (MCStudio) for Digital Signal Controllers (DSC) – MC-24R and MCT-01



SW Tools
&
Application Software Library
&
algorithms

Experiment in compatibility European/Russian SpaceWire implementation



STAR –Dundee SpaceWire USB Brick

Up to 10m, up to 200 (400Mbps)

ELVEES SpaceWire MCT-01 module

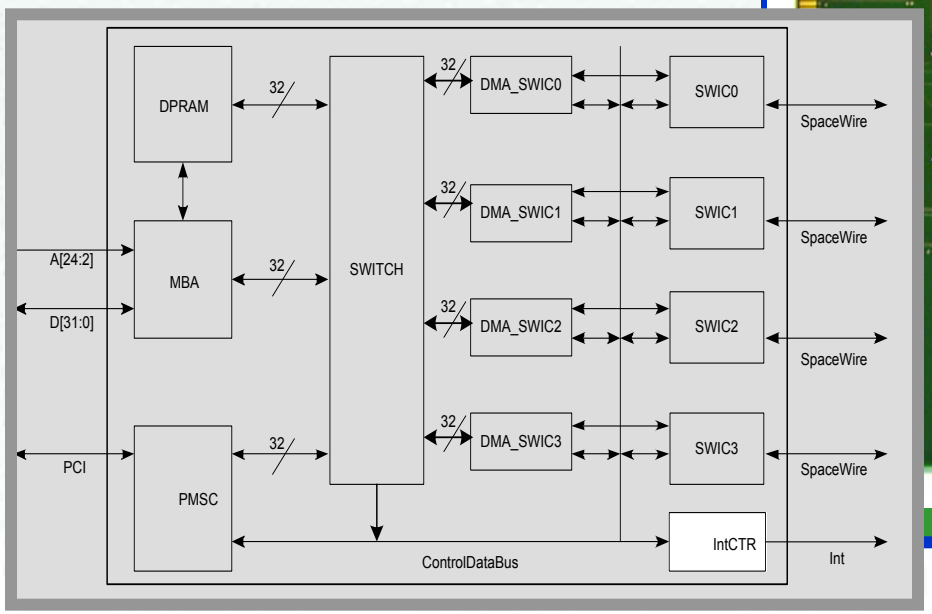
MCB-01 Multichannel Adapter of the packet data transmissions

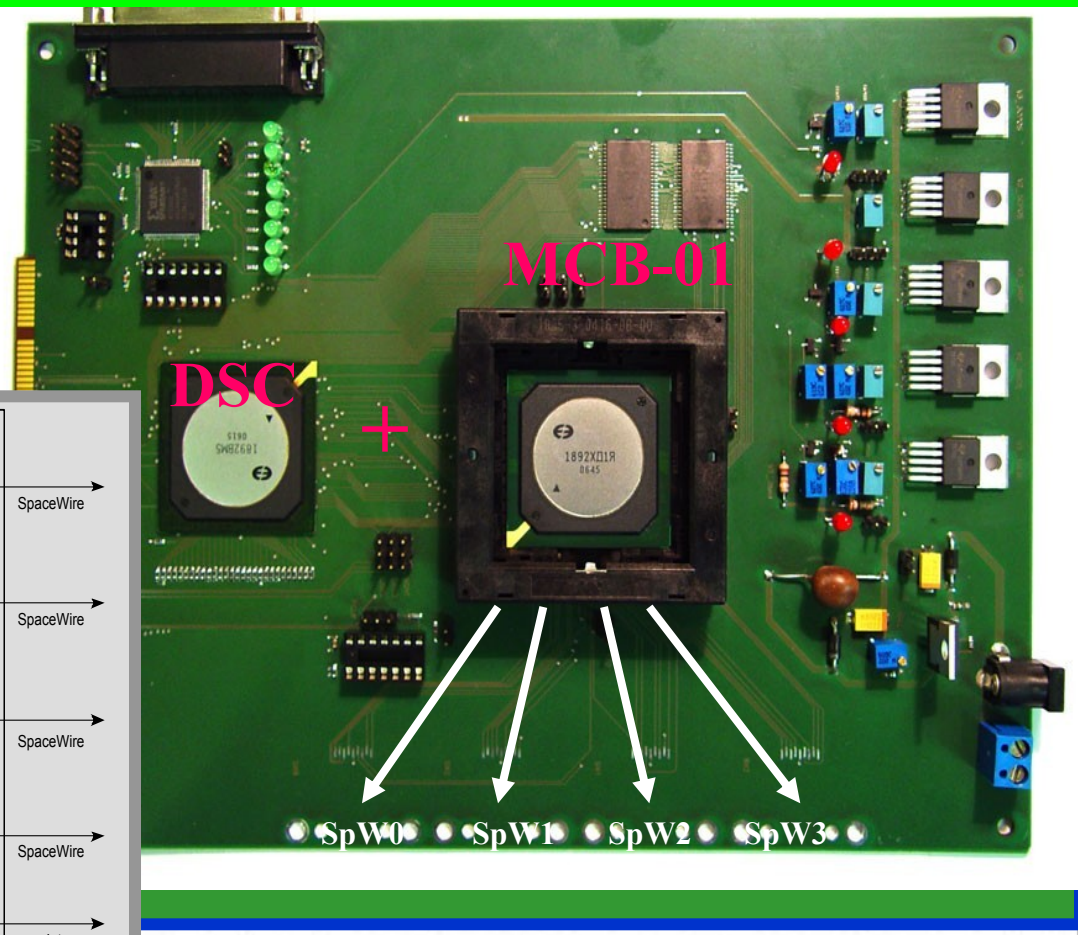
- 250 nm;
- 4 channel SpaceWire, ECSS-E-50-12A standard;
- data rate – 2 – 400 Mbps thought the cables and connectors specified by standard;
- embedded LVDS ANSI/TIA/EIA-644(LVDS) transceivers;
- PCI (32 bit/33-66 MHz), Local Bus Specification. Rev. 2.2.;
- 32b parallel port to Multicore chipset or others processors;
- embedded SRAM, 2Мбит (64KWx32b)
- package - HSBGA416 (for the engineering samples)

MCB-01 - 4-channels SpaceWire/PCI adapter for MultiCore Chipset enhancement

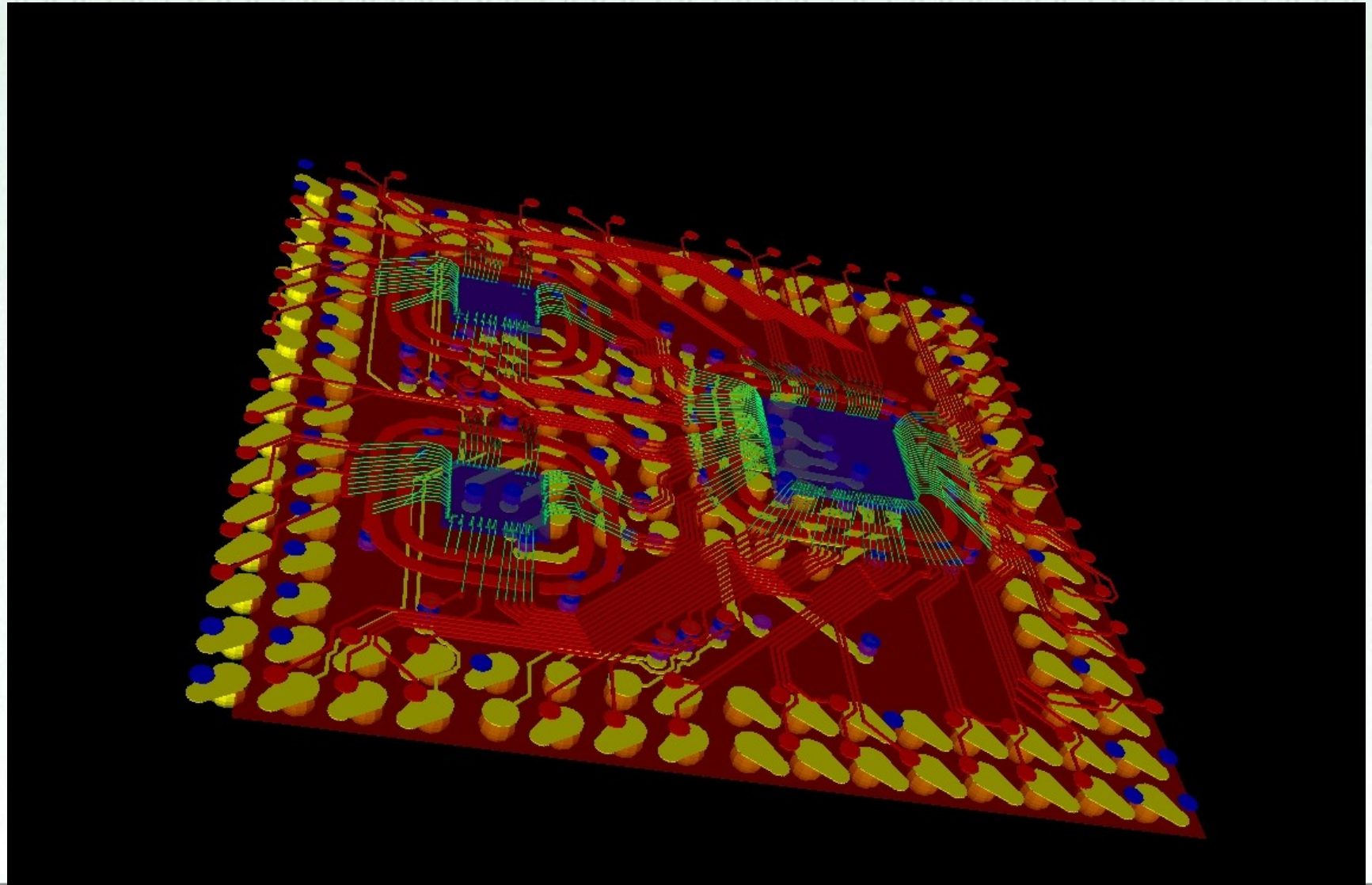
1.5 GFLOPs 4-Channel Processor Element with SpaceWire Links

+

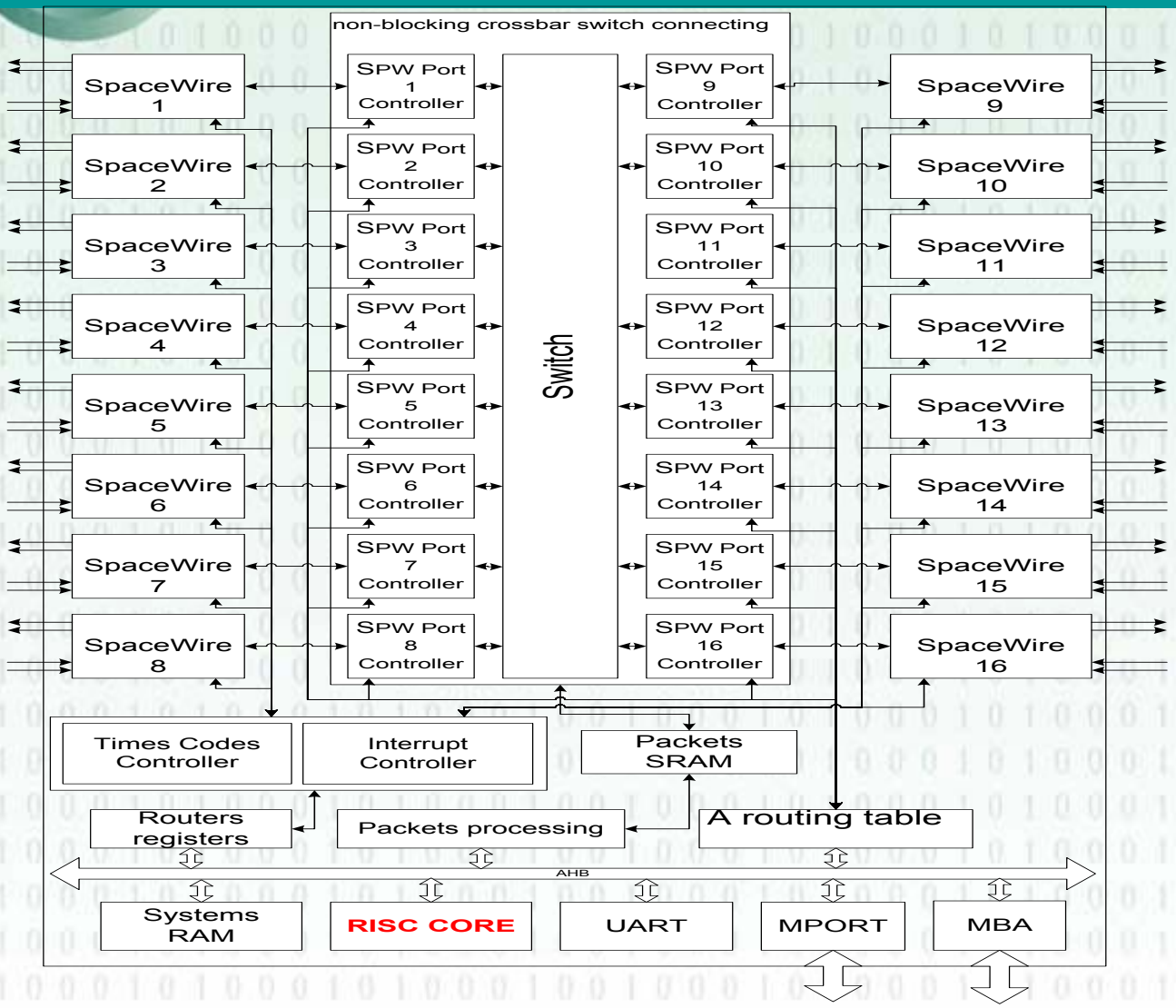


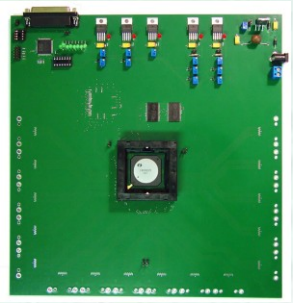


ELVEES SIP technology for joining Multicore chips without SpaceWire links with MCB-01 IC Plus ADC/DAC IC Plus Memory IC



МСК-01 (1892ХД2Я)-
16-channels SpaceWire Router with embedded RISC-Core





4GB SDRAM

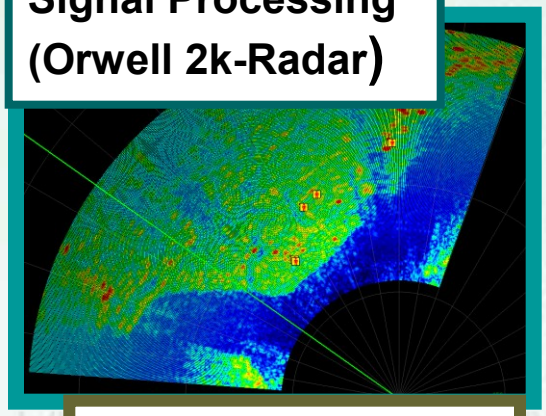
MCK-01 parameters (preliminarily)

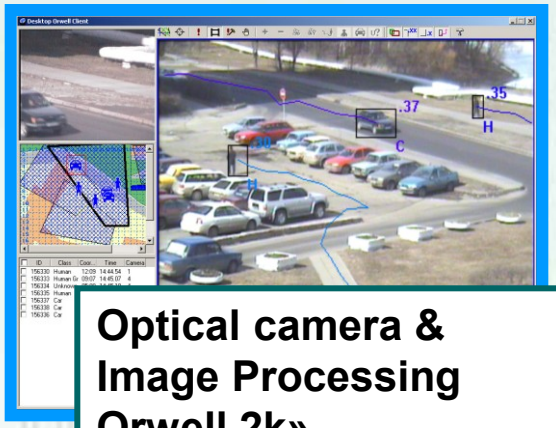
- 0.25-um;
- 16 channel SpaceWire, ECSS-E-50-12A standard;
- data rate – 2 – 400 Mbps thought the cables and connectors specified by standard;
- support of signal, symbol exchange, packet and network stack protocols of SpaceWire;
- Multicast/broadcast support
- embedded LVDS ANSI/TIA/EIA-644(LVDS) transceivers;
- embedded MIPS32 compatible RISC core (based on “MULTICORE” IP library) used for the configurable port service and administration of communication networks;
- 32 bit parallel port for “MULTICORE” chipset connections or for the additional external memory;
- Embedded RAM (25 Kbytes): program and data memory for RISC core (16 Kbytes), packet memory (8 Kbytes), routing memory (1Kbytes);
- Radiation Tolerant for aerospace applications
- package - HSBGA416 (for the engineering samples)

ELVEES's technologies for the MCFlight Space Wire based Image & Signal processing aerospace systems

ELVEES's "fusion sensors" programmable platform

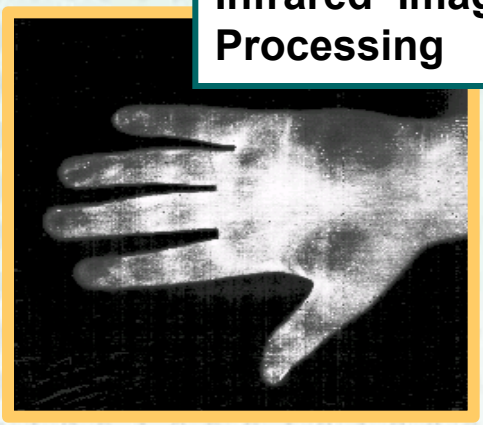
Signal Processing (Orwell 2k-Radar)



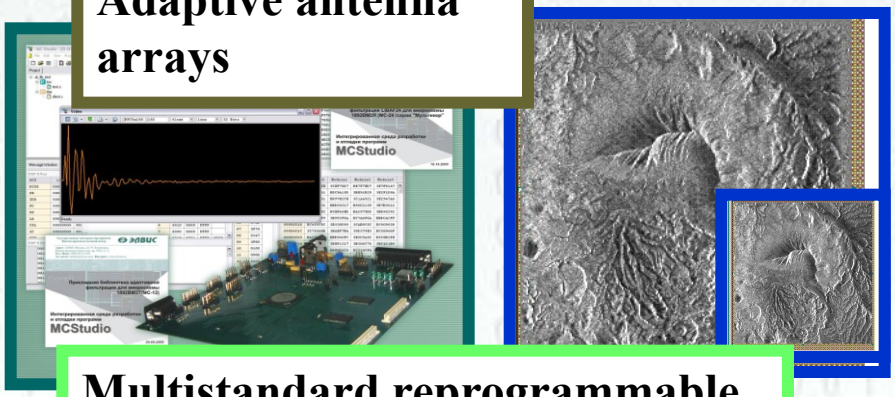


Optical camera & Image Processing Orwell 2k»

Infrared Image Processing

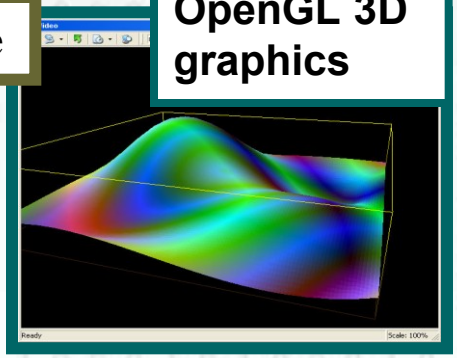


Adaptive antenna arrays



Information security gate

OpenGL 3D graphics



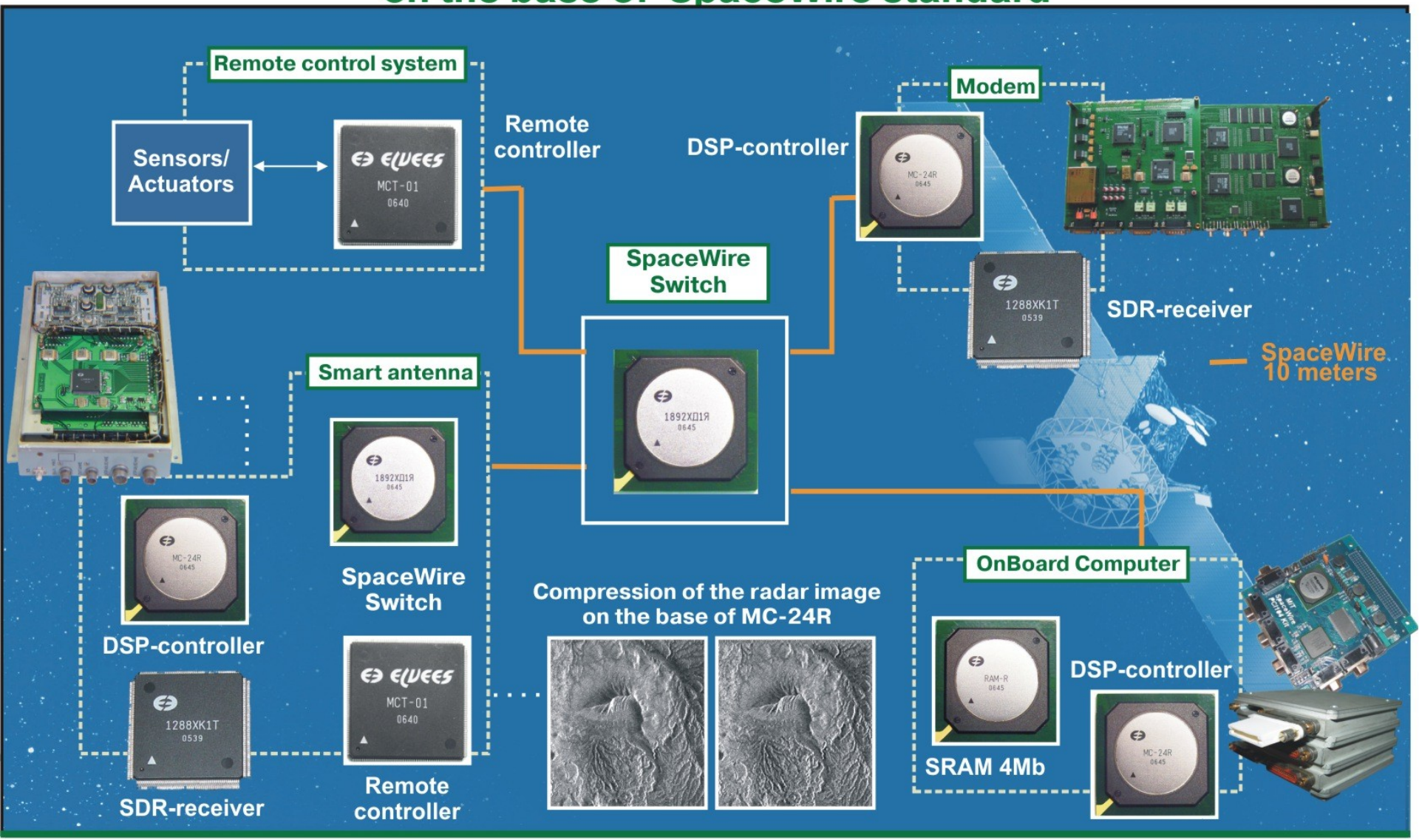
Multistandard reprogrammable

Global positioning and telecommunications chipset

"Soft Defined Radio" based "MultiFlex" chip

“MULTICORE" - RUSSIAN INNOVATIVE VLSI DESIGN PLATFORM

Unified aerospace board on the base of SpaceWire standard



ELVEES

R&D center “ELVEES”

multicore.ru

RnD “SUBMICRON” Company

On-board processing system

❑ 4 reconfigurable processing channels on the 16 Multicore SpaceWire Signal microprocessor MC-24R;

❑For one Channel:

✓100 MHz Clock;

✓ 2.4 GFLOPs (IEEE 754);

✓ 6.4 GOP s (16b);

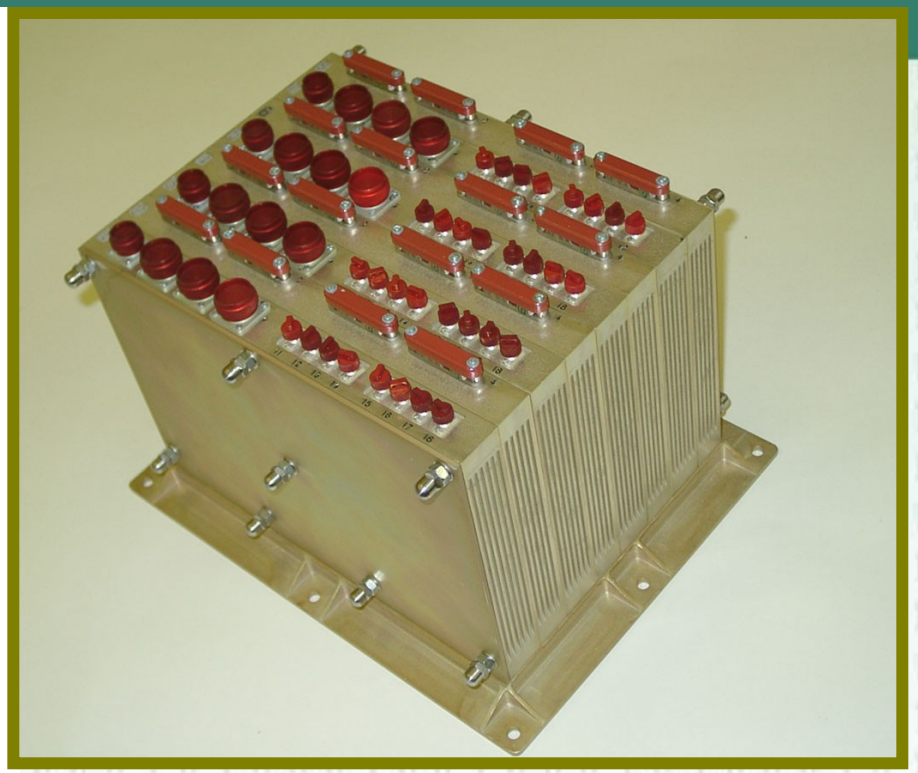
✓ 2 GB Data/Program SDRAM;

✓ 16 MB Program Memory(FLASH);

❑Interfaces:

• 2 IEEE1553;

•The channel of telemetry



6U form factor

Power - < 60W

Voltage - 27±1,5V

Sizes (mm): 323x245x197

Weight: < 8kg.

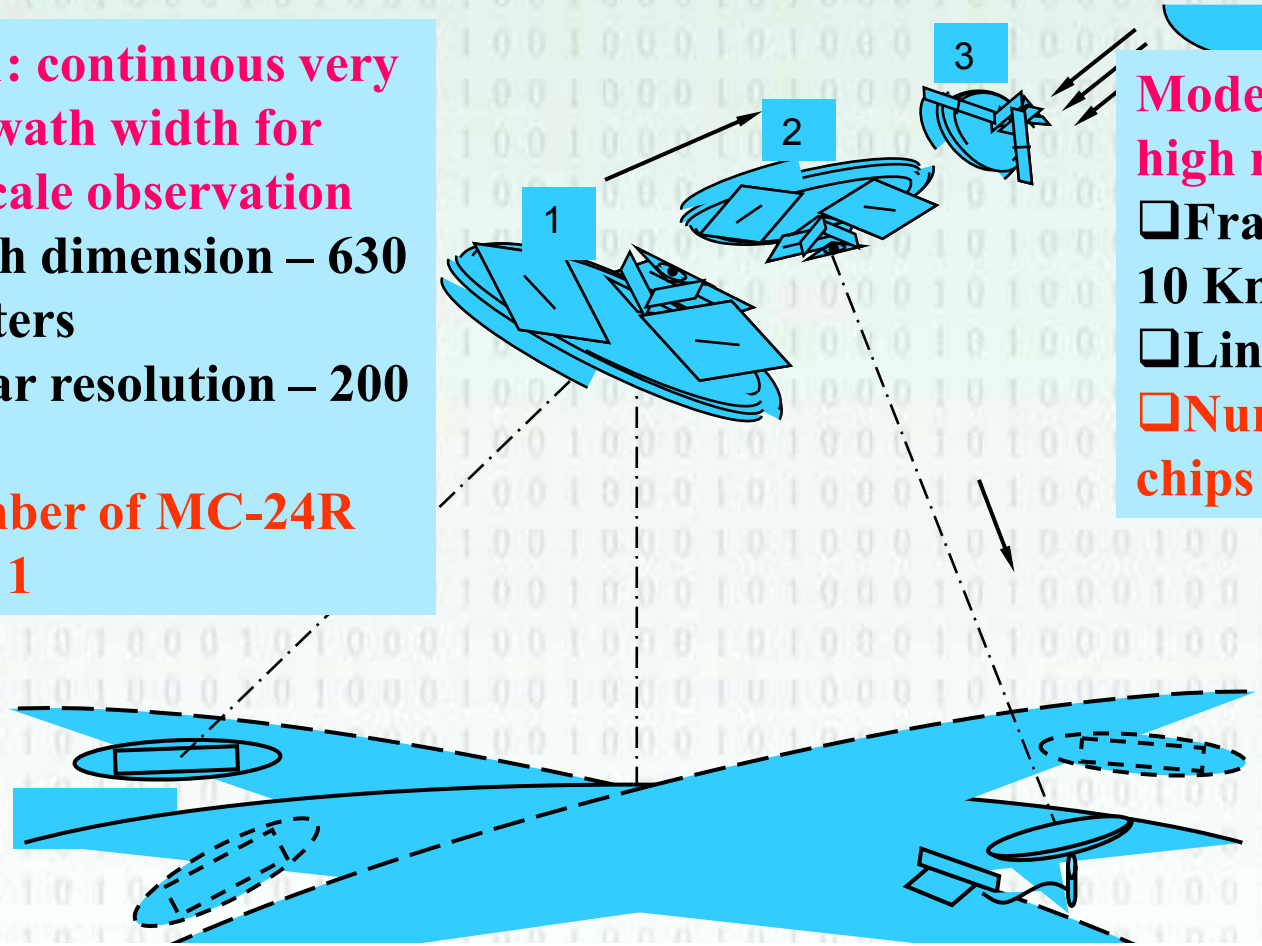
SMALL SATELLITE BASED RADAR WITH ON-BOARD IMAGE SYNTHESIS FOR ECOLOGICAL MONITORING ON THE MCFlight SPACE WIRE CHIPSET

Mode 1: continuous very large swath width for large scale observation

- ❑Width dimension – 630 kilometers
- ❑Linear resolution – 200 meters
- ❑ Number of MC-24R chips – 1

Mode 2: separate frames, high resolution

- ❑Frame dimension – 10 Km x 10 Km
- ❑Linear resolution – 3m
- ❑Number of MC-24R chips – 8



1 – SAR monitoring; 2. The Real Time results transferring to the MULTICORE based Ground station;

SpaceWire applications in the projects of the Institute Of Space Research, Russian Academy of Science:

- The MGNS instrument for the BepiColombo mission.
- The space scientific project SPECTR-UF, (Russian Space Programme-2015);
  SpW in on-board mass memory for storing scientific data.
- The space scientific project SPECTR-RG, (Russian Space Programme-2015);
  SpW as the main instruments payload interconnection (Lobster(UK), Calorimeter (USA-Japan-Holland).
- Instruments BIUS, ART-XC.
- Also considered for:
  - ✓ eRosita (Germany)
  - ✓ Resonance (Russian Space Programme-2015), SpW as the main instruments payload interconnection.

Conclusions (1)

- The engineering samples of the MCFlight - "MULTICORE" platform and SpaceWire links based chipset (250 nm) with SpaceWire links for distributed aerospace systems have been received and its functionality is proved on the HW modules;
- ASICs and FPGA SpaceWire Links provide up to 400 Mbps and higher throughput (>5m) in the cross modules connections;
- Chipset provides a lot of the innovational features and supports high performance, programmability, scalability and the flexibility For the fault-tolerance distributed systems with the integrated architecture
- A lot of ELVEES 's technologies for "MULTICORE" platform (SDR, Adaptive signal/image processing , 3D graphics , Networks information security, multimedia, Intellectual systems of video observation) will be transferred on the MCFlight chipset;

Conclusions (2)

- **Synthesizable MultiCore MCFlight RH oriented chipset can be easily modified (during some months) by others IP-cores platforms (for example, for SPARC LEON RISC core) or for others interfaces (Space Fiber) and put to the other design technologies (better nm CMOS or SOI).**
- **ELVEES &MIT are interested in cooperation with foreign firms and space agencies for the joint designing the chips and the space equipment, including for perspective systems of the space monitoring and telecommunication satellites.**
- **ELVEES R&D center offers for the ASIC/SOC Customers the full decision from the algorithms & chip up to the Embedded system & applied Software on the basis of the MULTICORE platform (MCFlight IC) or under the Customers requirements**

Thanks for your interest!

Questions?

ELVEES & MIT TEAM

Welcome to ELVEES & MIT for Cooperation

in above mentioned fields !